KATHOLIEKE UNIVERSITEIT LEUVEN
FACULTEIT INGENIEURSWETENSCHAPPEN
DEPARTEMENT ELEKTROTECHNIEK
Kasteelpark Arenberg 10, 3001 Leuven (Heverlee)

Distributed Amplification in CMOS

Jury:
Prof. Dr. ir. P. Moldenaers, voorzitter
Prof. Dr. ir. P. Reynaert, promotor
Prof. Dr. ir. M. Steyaert, promotor
Prof. Dr. ir. B. Puers
Prof. Dr. ir. B. Nauwelaers
Prof. Dr. ir. P. Leroux
Prof. Dr. ir. P. Wambacq
Prof. Dr. ir. J. Bauwelinck

Proefschrift voorgedragen
tot het behalen van de
graad van Doctor in de
ingenieurswetenschappen

door

Brecht Machiels

July 2012

D/2012/7515/65

ISBN 978-94-6018-529-8

"Disappointment is the nurse of wisdom."

Sir Boyle Roche

Voorwoord

Zonder goed te weten waar ik aan begon, heb ik ongeveer vier jaar en zeven maanden geleden mijn doctoraatsstudies aangevat. Al gauw werd mijn initiële enthousiasme wat getemperd door een, tot op heden nog steeds onverklaarbaar, probleem met het eerste versterkerprototype. Op miraculeuze wijze werkte het tweede prototype wel, met mooie resultaten, wat het allemaal weer wat aangenamer maakte. Hoewel er later nog enkele tegenslagen volgden, kijk ik met een goed gevoel terug op mijn tijd bij MICAS. Gedurende de doctoraatsopleiding, maar ook in de aanloop ernaar, hebben vele individuën in meer of mindere mate mijn werk en leven daarbuiten beïnvloed, en ik wil ze hier dan ook graag bedanken.

In de eerste plaats dank ik mijn promotoren, Patrick en Michiel, om mij de kans te geven om een doctoraat aan te vatten en mij vrijwel carte blanche te geven met betrekking tot mijn onderzoeksfocus. Die vrijheid waardeer ik erg, en daar heb ik dan ook gretig gebruik van gemaakt. Juist door die vrijheid was mijn werk echter misschien niet voldoende gericht op de heilige graal van de academische wereld, het produceren van zo veel mogelijk publicaties, maar desondanks ben ik er wel van overtuigd dat ik zeer veel technische kennis heb opgedaan door mijn eigen werk en door interacties met collegas. Ook bedankt, Patrick, voor de erg behulpzame technische discussies, vooral in de beginfase van het doctoraat. Bovenvermelde vrijheid is mede mogelijk gemaakt door financiering met een IMEC-beurs de eerste vier jaren, en het (laat het ons houden op een) misverstand dat hier rond bestond. Dank aan beide partijen om mij niet bij deze discussie te betrekken.

Verder dank ik de leden van mijn jury, prof. Bob Puers, prof. Bart Nauwelaers, prof. Paul Leroux, prof. Piet Wambacq en prof. Johan Bauwelinck, voor het nalezen van het proefschrift en het aanreiken van verbeteringen. Dank aan de voorzitter van de jury, prof. Paula Moldenaers, voor de vrijgemaakte tijd.

Ik dank ook het technisch personeel van ESAT, zonder wie een doctoraat een heel pak moeilijker zou zijn; Frederik, Noëlla, Thomas, Luc, Ludo, Jan, Sven en Rudi. Ondanks de Linux-omgeving viel het gebruik van de computerinfrastructuur op ESAT al bij al nog mee, dankzij de inspanningen van Stef, Rik, Piet, Marc, Frank en Ben. Daniëlle, Chris en Lut hebben mij onder andere ondersteund bij het verwerken van de vele formulieren. Als laatste dank ik twee personen die vaak onterecht worden vergeten in het dankwoord; Erwin en Jo van Europractice voor de, over het algemeen, zeer goede dienstverlening.

Voor expertise over onderwerpen buiten de traditionele MICAS-kennis ben ik al eens met een al-dan-niet domme vraag op zoek gegaan naar een slachtoffer in het gebouw. Zo ben ik door professoren Dominique Schreurs, Patrick Wambacq, Guy Vandenbosch, Emmanuel Van Lil en Joos Vandewalle hartelijk ontvangen. Also the expertise of Ilja, Majid and Vahid of TELEMIC has helped me more than once.

Over the years, I have shared an office with quite a number of people: Peter, Hans, Tom, Xu, Noël, Ying, Dixian, Shailesh and Iman. Thank you for the countless interesting discussions, both technical and non-technical, and not making too many irritating noises. I also enjoyed learning a little about Chinese, Indian and Iranian culture. A special no thanks to whoever is responsible for the ELECTA engines above our offices for the maddening noise and vibrations.

En dan nu het meest geanticipeerde deel van dit dankwoord, waar de MICAS-collegas gretig op zoek gaan naar hun naam, waarna ze vervolgens tevreden het boekje toeslaan, of het lichtjes geïrriteerd weggooien. Alvast mijn excuses aan de mensen die bij deze laatste horen, maar misschien hebt u niet voldoende uw best gedaan om op te vallen? Hier gaan we dan. Ik dank de MICAS-collega's, en ook enkele andere mensen die ik bijna even vaak tegenkwam, voor de aangename sfeer in de ESAT-kelders en daarbuiten. Dank aan Elie voor het samen ontcijferen van die Poynting-vector-paper. Hans M. voor de absurditeit. Johan voor de tekening. Dimitri voor de vele doorbraken. Bo for continuing to amaze me. Hagen voor de letsels. Bram voor de verhitte discussies over Linux. Piet C. voor dat vleugje magie. Ben voor de laid-back IT-support. Frederik C. voor de opgewektheid. Hans D. voor het aanreiken van onderwerpen tijdens de pauzes en het kunstig illustreren van bepaalde details, maar ook voor het delen van de pijn. Nico voor de nervositeit. Piet VDW., Tom VB., Greet, Luc en Michiel voor de onvergetelijke e-mails. Noël voor de sausjes. Brecht F. voor de onbedoelde arrogantie. Stef voor de vele boeken. Ercan for the sarcasm. Lianming for the calculations. Christophe voor de games. Evelien voor de beach-volley. Wim D. voor de yoghurt. Shailesh voor de Indische gerechten. Pieter N. voor het gebruiken van de wiki. Tom R. voor de internetaankopen. Stefan voor zijn dankwoord. Frank voor het meisjesachtige gegiechel. Nele voor het logo. Dimitri, Ying, Hans, Jens, Jelle, Wouter, en vele anderen voor het sjotten. Bart voor het ontdekken van de relatie tussen Hans en Tom. Maarten T. voor de blog. Lianggong voor de integratie. Ying H. voor de vrolijkheid. Valentijn voor de ziekenhuis-verhalen. Pieter DW. voor de gelatenheid. Frank the T. voor WOW. Filip, Elie en Mike voor de kortstondige fotografie-rage. Nick voor de klassieke mannelijkheid. Koen voor het pokerface. Jorg voor *zijn* pokerface. Philippe voor de onvolledige dankmatrix. Wim V. voor het heimelijke vertrek.

Hier wil ik ook prof. Luc Bienstman bedanken om mij aan te moedigen mijn elektronica-studies verder te zetten na mijn studies bij GroepT. Uw grote inzet voor de studenten is mij altijd bijgebleven en is na al deze jaren nog steeds ongeëvenaard.

Graag bedank ik ook vrienden en familie, gewoon om er te zijn en mij te steunen te alle tijde. In het bijzonder mijn ouders; bedankt pa en ma voor mij alle kansen te geven en achter mij te staan in alles wat ik doe.

Als laatste, maar als voornaamste, kom jij aan de beurt, Veerle. Niemand heeft grondiger als jou mijn thesis nagelezen. Maar belangrijker was je grote geduld met mij op de drukkere momenten van het doctoraat, en eigenlijk gewoon in het algemeen. Na moeilijkere dagen kon ik ook steeds bij jou terecht. Bedankt voor alles.

Leuven, juni 2012

Samenvatting

De gedistribueerde versterker is een type versterker waarin een signaal in parallel wordt versterkt door een aantal transconductantie-elementen zoals vacuümbuizen of transistoren. Dit staat in contrast met de klassieke gecascadeerde versterker, waar de versterkende elementen in serie staan. Een beperking van deze laatste is dat zijn versterkings-bandbreedteproduct inherent gelimiteerd is. De gedistribueerde versterker is niet onderworpen aan deze beperking; versterking kan worden uitgewisseld met vertraging, in plaats van met bandbreedte. Ten tijde van zijn uitvinding meer dan 70 jaar geleden werd de gedistribueerde versterker gebouwd met behulp van vacuümbuizen. Meer recent is er vernieuwde interesse voor de topologie sinds het mogelijk geworden is om monolithische gedistribueerde versterkers te produceren dankzij geïntegreerde circuittechnologie. Onderzoekers zijn er inmiddels in geslaagd om gedistribueerde versterkers te ontwerpen met bandbreedtes die 100 GHz overstijgen.

Een nadeel dat vaak aan de gedistribueerde versterker wordt toegewezen, wanneer ze vergeleken wordt met andere versterkertopologieën, is het hoge vermogenverbruik. Dit negatieve imago vindt gedeeltelijk zijn oorsprong in het feit dat gedistribueerde versterkers meestal worden ontworpen voor maximale versterking en bandbreedte, wat haaks staat op een laag vermogenverbruik. Het mag echter niet ontkend worden dat de topologie enkele karakteristieken heeft die de efficiëntie beperken. Zo gaat bijvoorbeeld de helft van de uitgangsstroom die wordt opgewekt door de versterkende elementen verloren. Daarom wordt het gebruik van de gedistribueerde versterker vaak niet overwogen voor laag-vermogen breedbandtoepassingen zoals in draadloze ontvangers.

In een eerste luik richt dit werk zich op de minimalisatie van het vermogenverbruik van de gedistribueerde versterker. Een eerste mogelijkheid om het vermogenverbruik te beperken bestaat erin het hierboven besproken verlies van de helft van het uitgangsvermogen te elimineren. Een gedistribueerde versterker met een *tapse uitgangstransmissielijn* laat toe dit te verwezelijken. Deze laatste heeft wel enkele nadelen, wat de toepasbaarheid ervan beperkt. Daarom wordt ze in dit werk in detail bestudeerd en wordt een *nieuw taperingschema* voorgesteld dat de beperkingen van het klassieke schema overwint. Daarnaast wordt aangetoond dat twee of meer gedistribueerde versterkers kunnen worden "gestapeld" om zo te kunnen baten van de multiplicatieve versterking die we ook terugvinden in gecascadeerde versterkers. Dit leidt tot een nieuwe versterkertopologie, de *tapse matrixversterker*. Het vermogenverbruik van deze wordt uiteindelijk nog verder teruggebracht door het toepassen van enkele generische laag-vermogentechnieken.

Teneinde de voorgestelde concepten te valideren werd een prototype 2×2 tapse matrixversterker ontworpen voor een 90 nm CMOS technologie. De specificaties van het prototype omvatten een versterking van 16 dB over een frequentieband van 22 GHz

en een vermogenverbruik van slechts 13 mW. De verhouding van het versterkingsbandbreedteproduct tot het vermogenverbruik van het prototype vestigt een nieuw record in de literatuur. De benodigde IC-oppervlakte van 0,31 mm^2 is zeer klein voor een versterker met deze performantie. Het gemiddelde ruisgetal in de 22 GHz brede doorlaatband bedraagt 5,4 dB, wat vergelijkbaar is met deze van andere breedbandversterkers in de literatuur. Enkele van de laag-vermogen ontwerpkeuzes, samen met de grote versterking, gaan wel ten koste van de lineariteit; het prototype toont een gemiddelde IIP3 van -7,3 dBm.

In een poging om de lineariteit van het prototype te verbeteren werd het ontwerp opnieuw geëvalueerd. Er wordt getoond dat de IIP3 kan worden verhoogd met ongeveer 10 dB door het verhogen van de stuurspanning van de transistoren in de tweede trap. Dit gaat echter gepaard met een sterk verhoogd vermogenverbruik. Door toepassing van resistieve degeneratie kan het vermogenverbruik worden teruggebracht tot 22 mW. Dit *ontwerp met een verhoogde lineariteit* illustreert dat de tapse matrixversterker in staat is tot het leveren van een zeer lineaire, grote versterking bij een laag vermogenverbruik, en is daarom een goede keuze voor laag-vermogen breedbandtoepassingen.

Een tweede luik in dit werk bestudeert de *reizende-golf-transistor*. Hoewel aanvankelijk geconcipiëerd als een continue versie van de gedistribueerde versterker, werd ontdekt dat ze in staat is om een tweede werkingsmodus te ondersteunen. Waar een signaal langs een transmissielijn energie verliest volgens een exponentiele wet, is de reizende-golf-transistor in staat een exponentieel groeiende golf te geleiden. In deze werkingsmodus wordt de maximale versterking van de transistor niet beperkt door verliezen zoals in een klassieke gedistribueerde versterker; door eenvoudigweg de breedte van de transistor te vergroten kan de versterking onbeperkt worden verhoogd. Om inzicht in deze werkingmodus te verwerven wordt de reizende-golf-transistor gemodelleerd als een actieve transmissielijn, wat het identificeren van de vereisten om een groeiende mode te verkrijgen vereenvoudigd. Dit model wordt dan gebruikt in het ontwerp van een *groeiende-golf-versterker*, een discrete implementatie van een reizende-golf-transistor, in CMOS. Het blijkt echter alles behalve eenvoudig om een groeiende mode te bekomen door de beperkingen van de CMOS technologie. Om deze te overwinnen wordt het kruis-gekoppelde transistorpaar geïntroduceerd in de versterker, wat het verkrijgen van de groeiende mode sterk vereenvoudigd.

Door zijn longitudinaal-reciproke karakter is de reizende-golf-transistor zeer gevoelig voor oscillaties. Hoewel bewezen dat stabiliteit kan gegarandeerd worden door een zeer goede terminatie van de transistor, is dit niet mogelijk in een realistische omgeving. Daarom worden er in dit werk methodes onderzocht om niet-reciprociteit in te brengen in de versterker. Eén optie bestaat erin gebruik te maken van meta- of magnetische materialen. Omdat deze materialen echter niet beschikbaar zijn in standaard CMOS processen, wordt het ontwerp van een discrete niet-reciproke groeiende-golf-versterker aangevat. De eerste simulaties van een eenheidscel bestaande uit een spoel, een condensator en een NMOS transistor tonen aan dat een stabiele versterking inderdaad kan bekomen worden.

Abstract

A distributed amplifier is an amplifier in which a signal is amplified in parallel by a number of transconductive devices such as vacuum tubes or transistors. This is in contrast to the classic cascade amplifier, in which the amplifying devices are connected in series. A limitation of the latter is that its gain-bandwidth product is inherently limited. The distributed amplifier is not subject to the same limitation; gain can be traded for delay, instead of for bandwidth. At the time of its conception over 70 years ago, the distributed amplifier was built using vacuum tubes. More recently, the topology has found renewed interest due to the ability to produce monolithic distributed amplifiers using integrated circuit technology. Researchers have since managed to design distributed amplifiers with bandwidths exceeding 100 GHz in modern RFIC technologies.

A disadvantage often attributed to the distributed amplifier, when compared to other amplifier topologies, is its high power consumption. While part of this high-power image stems from the fact that distributed amplifiers are typically optimized for maximum gain and bandwidth, automatically leading to a high power consumption, it is true that the topology has some characteristics that limit its efficiency. For example, in its basic configuration, half of the output current generated by the transistors is essentially lost. For these reasons, the distributed amplifier is often quickly dismissed for use in low-power broadband applications such as in wireless receivers.

In a first part, this work focuses on the minimization of the distributed amplifier's power consumption. A first opportunity in reducing the power consumption involves eliminating the loss of half of the output current mentioned above. A distributed amplifier with a *tapered output transmission line* allows to do just this. However, the latter suffers from a number of disadvantages, limiting its use. To this end, the tapered distributed amplifier is analyzed in detail and a *new tapering scheme* is presented that overcomes the limitations of the classic scheme. In addition, it is shown that two or more tapered distributed amplifiers can be stacked in order to enjoy the increase in gain-to-power ratio of cascaded amplifiers. This leads to the new *tapered matrix amplifier* topology. Finally, the latter is enhanced with a number of generic low-power techniques to further reduce its power consumption.

To validate the presented concepts, a prototype 2×2 tapered matrix amplifier was developed in a 90 nm CMOS technology. The specifications of the prototype include a gain of 16 dB across a 22 GHz frequency band and a DC power consumption of only 13 mW. This gain-bandwidth to power consumption ratio presents a new record. The occupied die area of 0.31 mm^2 is very small for an amplifier with these specifications. The average noise figure across the 22 GHz pass-band is 5.4 dB, and holds up very well compared to other broadband amplifiers in literature. Some of the low-power design

choices and the high gain do come at the expense of linearity however; the prototype shows an average IIP3 of -7.3 dBm.

In an attempt to improve the linearity of the prototype, its design was revisited. It is shown that IIP3 can be boosted by 10 dB by increasing the overdrive voltage of the second-stage transistors, but at the cost of a steeply increased power consumption. Introducing resistive degeneration, the power consumption can be reduced to 22 mW, also reducing the gain to 14 dB. This *linearity-enhanced design* illustrates that the tapered matrix amplifier is capable of highly-linear, high-gain amplification at a low power consumption, and is therefore an excellent choice in low-power broadband applications.

A second part of this work concerns the *traveling-wave transistor*. First conceived as a continuous version of the distributed amplifier, it was discovered that it is capable of supporting a second mode of operation. Where the signal on a lossy transmission line loses energy according to an exponential law, the traveling-wave transistor is capable of supporting an exponentially growing wave. In this operating mode, the maximum gain of the device is not limited due to losses as is the case in the classic distributed amplifier; by increasing the width of the device, the gain can be increased indefinitely. To gain insight in this mode of operation, the traveling-wave transistor is modeled as an active transmission line, which helps to identify the requirements necessary for obtaining the growing mode. This model is then used in the design of a *growing-wave amplifier*, a lumped approximation of the traveling-wave transistor, in CMOS. It is discovered that it is anything but straightforward to obtain a growing mode due to limitations of the CMOS technology. To overcome these limitations, a cross-coupled pair is introduced into the amplifier, which significantly facilitates obtaining the growing mode.

Due to its longitudinally reciprocal nature, the traveling-wave transistor is prone to become unstable. While it is shown that it is possible to maintain stability by proper termination of the device, this is not feasible in a realistic setting. For this reason, methods to introduce non-reciprocity are investigated. One option is to make use of the properties of meta- and magnetic materials. As these materials are not available in standard CMOS processes, design of a lumped non-reciprocal growing-wave amplifier is attempted. Initial simulations employing a unit cell consisting of an inductor, a capacitor and an NMOS transistor show that stable amplification can indeed be obtained.

List of Abbreviations and Symbols

Abbreviations

BEOL	Back End Of Line
BiCMOS	Bipolar CMOS
BJT	Bipolar Junction Transistor
BSIM	Berkeley Short-channel IGFET Model
BW	Bandwidth
CMOS	Complementary Metal Oxide Semiconductor
CPW	Coplanar Waveguide
CSSDA	Cascaded Single-Stage Distributed Amplifier
DA	Distributed Amplifier
DC	Direct Current
DLNA	Distributed LNA
DUT	Device Under Test
EM	Electromagnetic
FET	Field Effect Transistor
GBW	Gain-Bandwidth product
GSG	Ground-Source-Ground (probes)
GWA	Growing-Wave Amplifier
IC	Integrated Circuit
ICP	Input-referred 1 dB Compression Point
IIP3	Input-referred 3rd-order Intercept Point
LNA	Low-Noise Amplifier
MESFET	Metal Semiconductor Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MTL	Multiconductor Transmissions Line
NF	Noise Factor
NMOS	n-channel MOSFET
OIP3	Output-referred 3rd-order Intercept Point
PCB	Printed Circuit Board
PNA	Programmable Network Analyzer
PSD	Power Spectral Density
RF	Radio-Frequency
RFIC	Radio-Frequency Integrated Circuit
SFG	Signal Flow Graph
SiGe	Silicon-Germanium
TL	Transmission Line
TMA	Tapered Matrix Amplifier

TWF	Traveling-Wave FET
UWB	Ultra Wideband
VNA	Vector Network Analyzer

Symbols and Quantities

$^+, ^-$	Superscripts indicating forward and reverse traveling-waves
$\Im$	Imaginary part of
$\Re$	Real part of
A_v	Voltage gain
B	Bandwidth (Hz)
C	Capacitance (F)
$\mathbf{C}$	Per-unit-length capacitance matrix
C_{gs}, C_{gd}, C_{ds}	MOSET gate-source, gate-drain and drain-source capacitances (F)
$\vec{E}$	Electric field vector
G	Power gain
F	Noise factor
$\mathbf{G}$	Per-unit-length conductance matrix
$\vec{H}$	Magnetic field vector
I	DC Current (A)
$\vec{J}$	Current density vector
L	Inductance (H)
$\mathbf{L}$	Per-unit-length inductance matrix
N	Number of distributed amplifier sections
P_{av}	Average power (W)
P_{DC}	DC power consumption (W)
R	Resistance (Ω)
$\mathbf{R}$	Per-unit-length resistance matrix
S	Output current multiplication factor
T	Time delay (s)
T_0	Absolute temperature
V	DC voltage (V)
V_{DD}	DC supply voltage
V_{GS}, V_{DS}	MOSET gate-source and drain-source bias voltages
$V(z)$	Voltage along a transmission line at coordinate z
W	MOSFET channel width (m)
Y	Admittance
$\mathbf{Y}$	Per-unit-length admittance matrix
Z	Impedance
$\mathbf{Z}$	Per-unit-length impedance matrix
Z_0	Characteristic impedance
Z_S	Source impedance
Z_L	Load impedance
a	Complex chirality parameter

b	Complex reciprocity parameter
a_k, b_k	Current and characteristic impedance tapering factors
d	Interval (m)
f_c	Cut-off frequency (Hz)
f_n	Natural frequency (Hz)
g_m	Small-signal transconductance gain of a BJT or MOSFET (S)
i_d	MOSFET AC drain current (A)
k	Boltzmann constant (J/K)
r_{ds}	Output resistance of a MOSFET
r_g	MOSFET gate resistance (Ω)
s	Complex Laplace variable
v	AC voltage (V)
v_{gs}	MOSET gate-source voltage (V)
Γ	Voltage reflection coefficient
$\mathbf{\Lambda}$	Diagonal eigenvalue matrix
α	Attenuation constant (np/m)
β	Phase constant (rad/m)
γ	Complex propagation constant
ζ	Damping ratio
θ	Phase of a complex number
μ	Edwards-Sinsky stability factor
π	The well-known constant
ω	Angular frequency (rad/s)

Table of Contents

Chapter 1

Introduction

This introductory chapter situates distributed amplification in a broader context. First, some application areas of broadband amplifiers are discussed and a short overview of the different integrated circuit technologies is given. The next section covers the various broadband amplifier topologies, discussing their advantages and disadvantages. Finally, a summary of the research and an outline of the text are given.

1.1 Applications of Broadband Amplifiers

What better way to start this introduction than to reference one of the classic theorems that lie at the basis of information theory? The Shannon-Hartley theorem [Cou97] provides an expression for the capacity of a channel subject to additive white Gaussian noise, that is, the theoretical limit on the rate of information that can be reliably transmitted over this channel. It states that the channel capacity C (bits/s) of a channel with a bandwidth B (Hz) and a signal-to-noise ratio S/N (W/W) is given by

$$C = B\log_2\left(1+\frac{S}{N}\right). \tag{1.1}$$

Unfortunately, the theorem does not say anything about how to build a communication system that has a channel capacity close to this limit. However, more recently, forward error-correcting channel coding techniques have been developed that closely approach the channel capacity, the so called turbo codes [Ber93].

Equation (1.1) implies that a large channel capacity can be obtained by increasing the bandwidth, even if the signal-to-noise ratio is low. Thus, the signal power S may be low as long as the bandwidth is large. **Ultra-wideband** (UWB) is an example of a radio technology that makes use of a large bandwidth to transmit data at a high bitrate in an efficient manner [Str03]. Figure 1.1 shows pulse-based UWB waveforms in the time and frequency domains. The short pulses distribute the energy across a large bandwidth. The energy in any small frequency band is small and therefore does not interfere with carrier-based communication. Compare this to traditional carrier-based systems, where all energy is concentrated in a small frequency band.

With the adoption of the 3.1 to 10.6 GHz band for unlicensed use of UWB across the globe, new applications such as Wireless USB have surfaced, allowing for short-range data transfer up to 480 Mbit/s. UWB in the 3.1-10.6 GHz band offers a major advantage

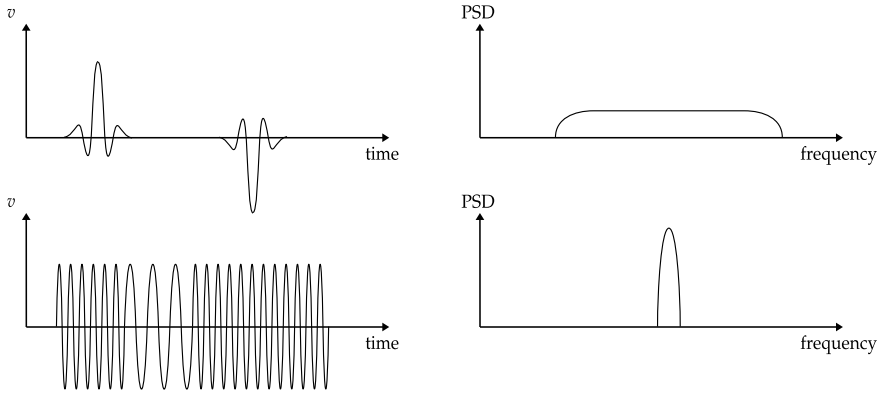


Figure 1.1: UWB (top) versus traditional carrier-based (frequency modulation, bottom) communication in the time and frequency domain.

over wireless millimeter-wave standards such as WiGig; the latter is limited to short-range (within a room) communication due to the high absorption of 60 GHz waves. Data communication at 60 GHz does enable significantly higher data rates, but this comes at the cost of a large power consumption. Finally, another interesting property of UWB is that it does not interfere with traditional narrowband communication standards in the same band since the radiated power is very low. Applications making use of the full 3.1-10.6 GHz UWB band require radio-frequency (RF) transmitter and receiver frontends capable of amplifying signals across the wide 7.5 GHz band. These broadband amplifiers should ideally be cheap and draw little power.

Broadband amplifiers can also be useful in **multistandard transceivers**. Today, there is a myriad of wireless standards: GSM (400, 450, 850, 900, 1800 and 1900 MHz), Bluetooth (2.4 GHz), Wi-Fi (2.4 and 5 GHz). Modern cell phones (smartphones) and portable computers (laptops, netbooks and tablets) typically need to support at least a number of these, often using a separate transceiver for each standard. Replacing these with a single generic transceiver can significantly reduce costs. Focusing on the low-noise amplifier in a multistandard receiver, there are several options to build a multistandard low-noise amplifier (LNA) [And03]. One amplifier topology that can be considered is the reconfigurable tuned LNA. However, the tuning range of an amplifier is inherently limited, not allowing the amplifier to support standards with frequencies that lie far apart. The more flexible alternative is the broadband amplifier.

Taking the multistandard transceiver concept one step further, one arrives at the concept of **cognitive radio** [Wan11]. This is a radio that aims to make efficient use of a wireless medium, while avoiding interfering with licensed users. To do this, the radio analyzes the state of the medium and distributes the gathered information to its peers. Based on this information, nodes can adjust their transmission and reception parameters to the required transfer speed of the link. This process is called the cognitive cycle, shown in Figure 1.2. **Software-defined radio** (SDR) is closely linked to the concept of cognitive radio, in which software algorithms analyze the state of the network and adjust the radio's parameters in response. To maximize the usefulness and performance of a

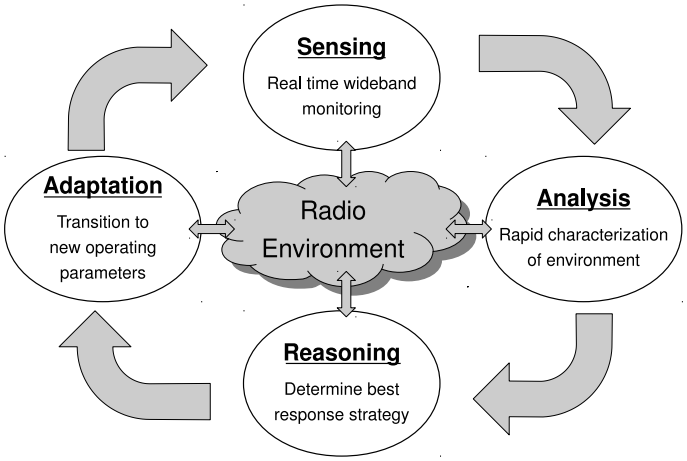


Figure 1.2: The cognitive cycle [Wan11].

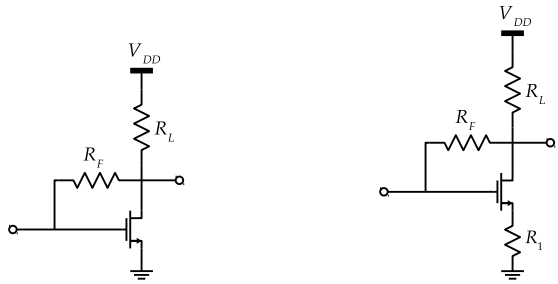
cognitive radio, it should be able to send and receive in a frequency band that is as large as possible, requiring the availability of broadband amplifiers.

1.2 Integrated Circuit Technology

These amplifiers, and other building blocks of transceivers, are typically implemented as an integrated circuit (IC). In contrast to amplifiers built from discrete components, IC implementations can be many times cheaper due to the reduction in manufacturing and material costs [Wik]. Additionally, they allow for miniaturization, an important feature in handheld consumer electronics where it frees up space for larger batteries.

Within the realm of integrated circuits, there are a multitude of possible technologies, which can be roughly divided into two categories. The first of these are the IC technologies designed specifically with the eye on RF applications. These include, for example, gallium-arsenide (GaAs), gallium-nitride (GaN) and indium-phosphide (InP) processes. The second category comprises silicon-based processes such as standard CMOS, silicon-on-insulator (SOI) and silicon-germanium (SiGe) BiCMOS. The silicon-based processes, and particularly standard CMOS, are decidedly inferior to the other group in terms of RF performance (gain, noise, power handling capability, etc.). However, CMOS has a single decisive advantage: low cost [Raz01]. This makes CMOS a very attractive option, even for RF applications, despite its sub-standard properties. Additionally, CMOS processes allow for integration with digital circuitry, eliminating the need for inter-IC communication and the associated costs. SOI and SiGe can compensate for some of the shortcomings of CMOS, but at an increased cost. For example, SiGe processes offer fast heterojunction bipolar transistors, making it more suitable for RF applications [Paw06].

Driven by this economic reality, there is a lot of research focused on RF circuit design in CMOS, pushing the limits of what is possible further and further. And this work is no



(a) (b)

Figure 1.3: A common-source amplifier (a) with resistive feedback, and (b) with both resistive feedback and degeneration.

exception; the ideas and circuits presented in this thesis have all been influenced by a CMOS mindset.

1.3 Overview of Broadband Amplifier Topologies

A broadband amplifier is characterized by its flat gain across a large frequency band. This typically requires having a good match across this bandwidth, something that is difficult to obtain due to the capacitive input impedance of a MOS transistor. Any attempt to match a transistor to a 50 Ω source inevitably means compromising gain, bandwidth or other factors, as implied by the Bode-Fano criterion [Poz05]. This trade-off can be made in a number of ways, as is apparent from the number of different broadband amplifier topologies which are briefly discussed next.

1.3.1 Resistive-Feedback Amplifier

Resistive feedback is a popular method for enhancing the bandwidth of a common-source amplifier [Lee04a]. Figure 1.3a depicts a basic resistive-feedback amplifier. The feedback resistor R_F provides shunt-shunt feedback [Raz01], which lowers the input and output impedances and allows obtaining simultaneous input- and output-matching in the case that the source and load impedances are equal [Lee04a]. The feedback also extends the bandwidth and desensitizes the properties of the amplifier from device parameters, in exchange for gain. The resistive-feedback amplifier can be degenerated to obtain the unfortunately-named[1] *shunt-series amplifier* shown in Figure 1.3b [Lee04a]. The degeneration resistance R_1 provides a second feedback loop that further extends the bandwidth of the amplifier.

The input and output capacitance of the transistor ultimately limit the bandwidth of the amplifier. For this reason, shunt peaking inductors are often used to maximize the bandwidth [Che07, Che09, Oku09]. Additionally, the degeneration resistance can be

[1] The name shunt-series does not identify the type of sense and return mechanisms of the feedback circuit, but instead refers to the combination of shunt (R_F) and series (R_1) feedback.

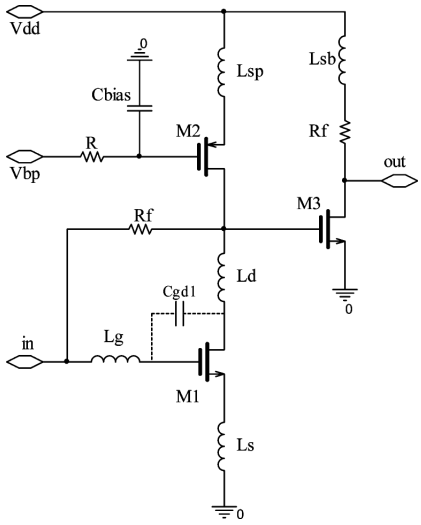


Figure 1.4: A resistive feedback amplifier with shunt peaking and inductive degeneration [Che09].

replaced with an inductor, which can also help to increase the bandwidth. Figure 1.4 shows a resistive-feedback amplifier with shunt peaking and inductive degeneration.

Strengths of the resistive-feedback amplifier include a low power consumption and a low area requirement. On the downside, the gain-bandwidth (GBW) product of the amplifier is closely linked to the unity current-gain frequency f_T of the transistor used and is therefore inherently limited. Voltage gain is typically boosted by increasing the impedance at the output node. To provide a match to 50 Ω, or to provide power gain, an output buffer can be included, but this adds significantly to the power consumption of the amplifier.

1.3.2 Filter-Match Amplifier

Another approach to broadband amplifier design embeds the input capacitance of the transistor into a bandpass filter network to provide a good input match [Bev04, Ism04], decoupling the latter from the transistor size. The use of a bandpass filter is however not suitable for applications which require amplification down to DC. As in the resistive-feedback amplifier, peaking inductors can be used to extend the bandwidth of the amplifier. Figure 1.5 shows an example of a filter-match amplifier. As the input filter requires additional inductors, the filter-match amplifier is less area-efficient than the resistive-feedback amplifier. The power consumption is comparable to that of resistive-feedback amplifiers, but the gain-bandwidth product is similarly limited.

1.3.3 Stagger-Tuned Amplifier

In a cascade amplifier, the stages can be tuned at different frequencies so that the net gain response is flat across the band [Lim03, Wu05]. Figure 1.6 shows how the

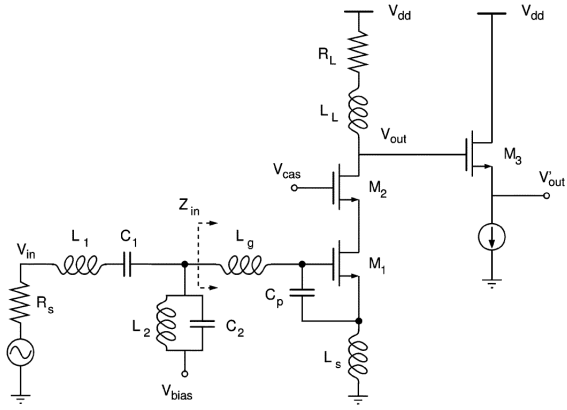


Figure 1.5: Inductively degenerated common-source amplifier with input matching filter [Bev04].

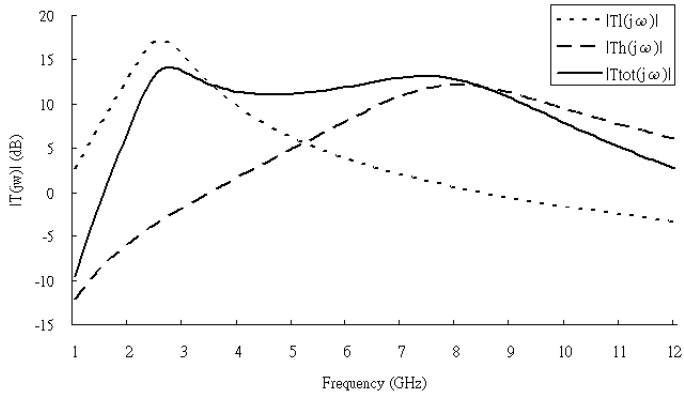


Figure 1.6: Stagger tuning: combining the narrow-band gain response of two stages into a flat broadband response [Wu05].

frequency responses of two stages combine to form a flat broadband response. This technique, stagger tuning, allows for a wider bandwidth than the resistive-feedback and filter-match amplifiers. However, some kind of filter network is required in addition to the stagger-tuned stages to provide a good input match, increasing the amount of die area required.

1.3.4 Balanced Amplifier

The balanced amplifier combines two identical amplifiers that operate 90 degrees out of phase, as shown in Figure 1.7. Quadrature couplers at the input and the output of the amplifiers take care of splitting the input signal into two signals that are 90 degrees out of phase and recombining the outputs of the amplifiers in phase respectively. In the ideal case where the amplifiers are identical and the quadrature couplers provide an exact 90

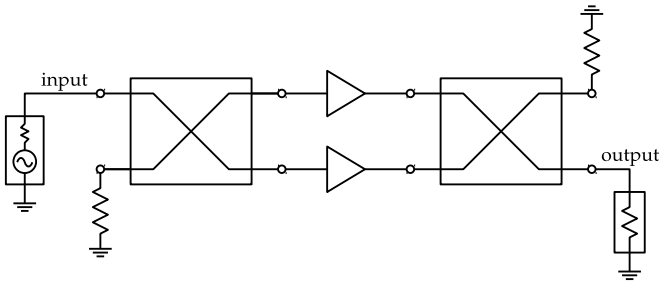


Figure 1.7: The balanced amplifier. Quadrature couplers at the input and output provide good matching.

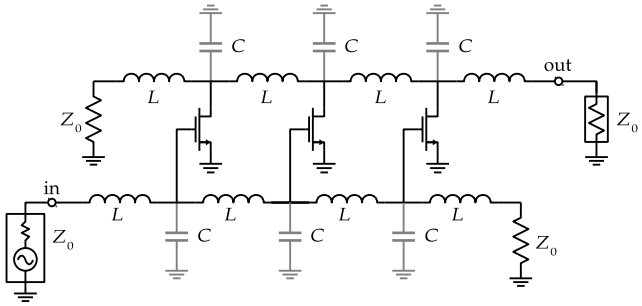


Figure 1.8: A three-cell distributed amplifier.

degree phase shift, reflections from the amplifier inputs cancel at the input to the coupler, resulting in a perfect input match [Poz05]. The reflected signals are dissipated in the resistively terminated isolated port. The same magic takes place at the output of the balanced amplifier. Amplifiers that have poor matching properties can thus be combined to provide good input and output matching. This allows the individual amplifiers to be optimized for gain, bandwidth and noise, without regard to input and output matching.

The bandwidth of the balanced amplifier is ultimately limited by the bandwidth of the coupler. Unfortunately, broadband (multi-section) couplers are very large and are not suited for monolithic integration. The gain of the balanced amplifier is equal to the average of the gains of the individual amplifiers, implying that the balanced amplifier is not as power-efficient as other amplifier topologies. Additionally, the resistor at the isolated port of the input coupler degrades the noise figure of the amplifier, limiting the minimum noise figure to 3 dB [Bev04].

1.3.5 Distributed Amplifier

The distributed amplifier takes a markedly different approach to broadband amplification. In contrast to the conventional cascade amplifier, transistors are placed in parallel. The parasitic input and output capacitances of the transistors are absorbed into artificial transmission lines (LC ladders), as shown in Figure 1.8. This topology allows breaking free from the classic gain-bandwidth limitation, as is explained next.

For a single transistor, the gain-bandwidth product is basically fixed. By doubling the transistor's width, its gain is doubled, but its bandwidth is halved due to the increased parasitic capacitance. In the distributed amplifier, the number of gain cells can be doubled, doubling the gain, but without degrading the bandwidth. This is because the parasitic capacitances of the different gain cells are not lumped together, but are separated by the transmission line sections. While the bandwidth is not affected, the time it takes for the signal to propagate from the input to the output is increased. In the distributed amplifier, gain can be exchanged for *delay* as opposed to for bandwidth, as is the case in a conventional amplifier [Lee04a]. Additionally, due to the fact that the source and load connect to terminated transmission lines, excellent wideband matching is inherent to the distributed amplifier. Finally, note that the number of gain cells can not be increased indefinitely due to losses in the transmission lines[2].

As the input signal travels down the input transmission line (the gate line), it sequentially excites the gain cells, which each inject a current into the output (drain) transmission line. This current splits up equally into a left-bound part and a right-bound part. If the delays between gain cells in the drain line match those in the gate line, the right-bound currents, which flow into the load, add in phase. The left-bound currents add incoherently and are disposed of in the left-hand termination resistor. This reveals a fundamental weakness of the distributed amplifier; half of the output current is essentially lost, severely impacting its efficiency. This means that, for a comparable gain-bandwidth product, a distributed amplifier consumes more power than the other broadband amplifier circuits. A second disadvantage of the distributed amplifier is the large area requirement due to the large amount of inductors required to implement the LC ladders.

The noise performance of the distributed amplifier is not easily weighted against that of other amplifier topologies. Near DC, the minimum noise figure is limited to about 3 dB due to the input line termination resistor. At higher frequencies, the noise figure is not restricted by a 3 dB lower bound.

1.4 Summary of the Research

From Section 1.3, it is clear that the distributed amplifier offers a number of major advantages over the other amplifier topologies. Its excellent broadband properties have enabled the realization of extremely broadband amplifiers. Distributed amplifiers have been presented boasting bandwidths nearing 100 GHz in CMOS [Tsa05, Liu05, Arb09, Kim04], and even exceeding 100 GHz in heterojunction processes [Aga98, Mas03, Bae06, Che10, Dup10]. The pursuit of ever-higher gain-bandwidth products has traditionally been, and still is, the main focus in distributed amplifier research.

Due to its high power consumption and large required die area, the distributed amplifier is often promptly dismissed for use in commercial, low-power applications such as, for example, broadband low-noise amplifiers. However, few efforts have been made to design distributed amplifiers optimized for these kind of applications. Zhang and Kinget [Zha06] were one of the first to seriously consider this idea. They make an interesting point in stating that exactly the pursuit of the highest possible GBW product

[2] This is discussed in detail in Section 2.2

has probably played a large role in fostering the bad reputation of distributed amplifiers with respect to power consumption, since GBW maximization and minimization of power consumption are opposite requirements. Their presented distributed low-noise amplifier was a first step in showing that distributed amplifiers are in fact suitable for use in low-power applications, if power consumption is carefully considered during the design.

The focus of the work presented in this thesis is to further reduce the power consumption of a distributed amplifier for given gain and bandwidth specifications. To this end, the various opportunities for reducing the power consumption, including variations on the distributed amplifier topology, are investigated. The combination of two of these low-power techniques leads to a new distributed amplifier topology, the tapered matrix amplifier. Combination of the new topology with the other low-power techniques brings the power consumption down to the level of resistive-feedback amplifiers, at the same time retaining the broadband properties typical of distributed amplifiers. In addition, the required die area for a tapered matrix amplifier can be much smaller than for a distributed amplifier featuring a similar gain and bandwidth.

To assess the performance of the proposed techniques, a prototype low-power tapered matrix amplifier was designed. The design of this prototype, however, is complicated by some practical considerations such as lumped-line approximations and parasitics of the circuit components. To be able to deal with the complexity these bring, a pragmatic approach employing circuit optimization is taken.

A second part of the research concerns the traveling-wave transistor. Next to the lumped implementation described in Section 1.3.5, researchers envisioned a continuous version of the distributed amplifier. A field-effect traveling-wave transistor would simply be a very wide field-effect transistor (FET) operating as a distributed amplifier. Where in the distributed amplifier the bandwidth is determined by the lumped capacitances of the gain cells, the traveling-wave FET's bandwidth is only limited by the transit time of the charge carriers. The maximum gain of the traveling-wave FET is still limited due to losses in the input and output transmission lines, as is the case in the lumped distributed amplifier.

However, it was discovered that the traveling-wave FET can support another mode of operation. This mode, whose existence is dependent on the presence of passive coupling between the input and output transmission lines, allows for exponential signal growth. Even though there were quite a number of publications on the matter, it remains vague what the conditions are for this exponentially growing mode to exist. Also, there are serious doubts as to whether a traveling-wave transistor supporting the growing mode can be operated in a stable way. This work deals with the modeling of a traveling-wave FET (TWFET) capable of supporting the growing wave, and more importantly, uncovering the requirements for exciting the growing mode. Also the stability of the device is investigated.

1.5 Outline of this Work

This text's body is split up into four chapters, three of which discuss the lumped distributed amplifier with a focus on low-power designs. A fourth chapter is devoted to the subject of the traveling-wave transistor. The contents of the chapters are as follows:

- *Chapter 2* forms a general introduction to the distributed amplifier. It covers the effects of losses and other parasitics on the operation of the distributed amplifier and its noise and linearity characteristics. Finally, variations on the distributed amplifier topology encountered in literature are discussed.
- *Chapter 3* presents a generalized theory of the tapered distributed amplifier, which doubles the output current of the distributed amplifier. Based on this theory, a new tapering scheme is presented that offers some advantages over the classic scheme. The noise in the tapered distributed amplifier is also analyzed. Finally, the new tapered matrix amplifier topology is introduced, as well as techniques to help further reduce the power consumption of the amplifier.
- *Chapter 4* discusses the design of a prototype tapered matrix amplifier, starting from the high-level design and descending into details about layout and optimization. The measurements of the amplifier are discussed and compared to the state of the art. Finally, the design is revisited with the eye on improving the linearity of the amplifier.
- *Chapter 5* starts with a bird's eye overview of the literature on the traveling-wave transistor. Next, the traveling-wave transistor is modeled, building up from a simple active two-conductor transmission line model. The two-conductor model assists in gaining insight into the operation of the growing mode. A more complex three-conductor model supports the design of a TWFET supporting a growing mode. Finally, the stability of the traveling-wave transistor is discussed.

Finally, *Chapter 6* draws general conclusions, lists the main contributions to the state of the art and puts forward some suggestions for future work.

Chapter 2

Distributed Amplification

The distributed amplifier was first conceived by Percival in 1936 [Per36], but it only received the attention it deserved after a publication by Ginzton et al. in 1948 [Gin48]. In the past decade, the distributed amplifier has found renewed interest since it has become possible to design fully integrated distributed amplifiers using high-Q passives, opening the door to the realization of very broadband microwave amplifiers.

This chapter starts off with an introduction to the basic operating principle of the distributed amplifier, followed by an in-depth analysis of the artificial transmission lines employed in distributed amplifiers. The impact of losses and transistor-parasitics is illustrated next. The noise performance and linearity of the distributed amplifier are discussed. Finally, a number of variations on the distributed amplifier topology found in the literature are reviewed.

2.1 Principle of Operation

In distributed amplifiers, transconductive gain cells (vacuum tubes or transistors) are operated in parallel, whereas in classic amplifiers gain cells are typically placed in series. The parallel gain cells are distributed along two transmission lines as shown in Figure 2.1. The inputs of the gain cells connect to the input transmission line (bottom) and the outputs connect to the output transmission line (top) at regular intervals. As a signal travels from left to right on the input transmission line, it excites each gain cell in succession and is finally dissipated in the termination resistor on the right. The output current of the gain cells flows into the output transmission line, equally splitting into forward- and reverse-traveling waves. Provided the signal delay T_D between the outputs of the gain cells equals the delay between the inputs, the forward waves add in phase. This coherent signal is the output of the amplifier. Conversely, the reverse waves add incoherently (out of phase) and are dissipated in the right-hand termination resistor. Due to the fact that the output signals of the gain cells add, the amplifier is said to provide *additive* gain as opposed to *multiplicative* gain provided by a cascade amplifier. The output voltage is thus linearly proportional to the number of gain cells in the distributed amplifier.

In a practical implementation of a distributed amplifier, the gain cells have parasitic input and output capacitances. In this text, focus is on monolithic distributed amplifiers in CMOS technology; further discussion will assume MOSFET gain cells. Figure 2.2 shows a distributed amplifier using MOSFET transistors. The parasitic input and output

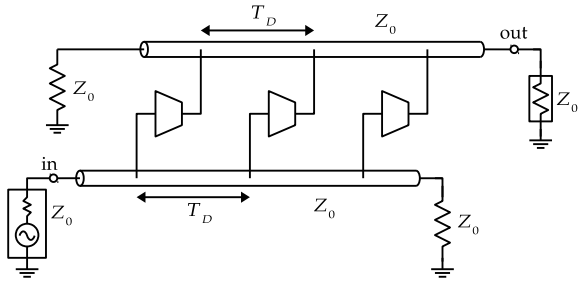


Figure 2.1: A distributed amplifier consisting of three gain cells.

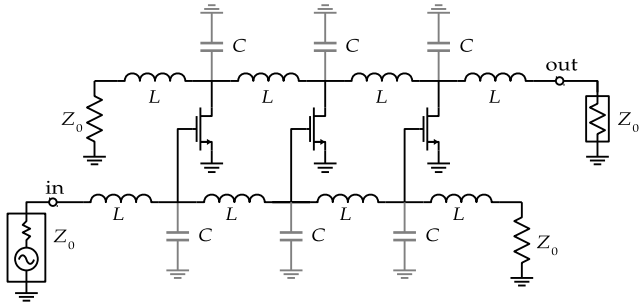


Figure 2.2: A distributed amplifier employing MOSFET gain cells and lumped inductors.

capacitances of the MOSFETs are displayed in gray. Together with the inductors, these capacitances form an LC ladder, approximating the transmission lines of Figure 2.1. The inductors separate the capacitors and therefore allow to place several transistors in parallel without suffering from a reduced bandwidth due to an accumulated lumped capacitance.

The voltage gain of the distributed amplifier can be readily determined to be

$$A_v = \frac{1}{2} N g_m Z_0, \tag{2.1}$$

where N is the number of gain cells and g_m is their transconductance. The factor $\frac{1}{2}$ is due to the fact that half of each gain cell's output current is lost in the left-hand termination resistor. The bandwidth of the amplifier is determined by the cut-off frequency of the LC ladders. The properties of LC ladders are discussed in the next section.

It is important to note that the input and output of the gain cells in a distributed amplifier are not power matched. In fact, most of the input power of the amplifier is dissipated in the termination resistor of the input line. As the signal travels down the input line, only a fraction of its energy is dissipated in the gain cells. This is in strong contrast with tuned amplifiers, where the input and output of transistors are typically power matched to obtain maximum power gain at the frequency of interest.

Comparing the distributed amplifier to the cascaded amplifier, we can identify some

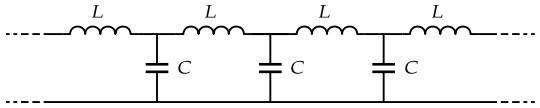


Figure 2.3: A short piece of an infinite LC ladder or lumped delay line.

obvious advantages and disadvantages. Due to its additive nature, a distributed amplifier can provide gain even if the gain of the individual gain cells is less than one. This allows selecting very small transistors, which have small parasitic capacitances, to maximize the bandwidth of the amplifier. Conversely, the additive gain makes it harder to obtain a large gain. The input and output impedance of the distributed amplifier are determined by the characteristic impedance of the transmission lines, which make broadband input and output matching easy to achieve. Finally, the distributed amplifier is basically a parallel power combiner, allowing it to generate a larger output power than what is possible using a cascade amplifier.

2.1.1 LC Ladders

One way to implement the transmission lines in a distributed amplifier is by means of LC ladders, in which the input and output capacitances of the gain cells provide the capacitance. In this section, the properties of LC ladders are investigated, and their influence on the distributed amplifier operation is discussed.

2.1.1.1 Characteristic Impedance

An LC ladder, shown in Figure 2.3, approximates a continuous transmission line. The difference with a continuous transmission line is visible in the frequency response of the ladder. For increasing frequencies, the LC ladder's behavior starts to deviate from that of the continuous line. An LC ladder's characteristic impedance[1] is given by [Lee04a]

$$Z_0 = \frac{j\omega L}{2}\left[1 \pm \sqrt{1 - \frac{4}{\omega^2 LC}}\right]. \tag{2.2}$$

The cut-off frequency of the LC ladder is defined as the frequency at which the characteristic impedance is purely imaginary and is given by

$$f_c = \frac{1}{\pi\sqrt{LC}}. \tag{2.3}$$

The delay of a single LC section is inversely proportional to the cut-off frequency:

$$T_D = \sqrt{LC}. \tag{2.4}$$

For frequencies below the cut-off frequency, $f = \alpha f_c$ with $\alpha \leq 1$, the term under the root in (2.2) is negative. To obtain a positive real part, we require the minus sign in

[1] The characteristic or surge impedance is defined as the input impedance of a transmission line of infinite length.

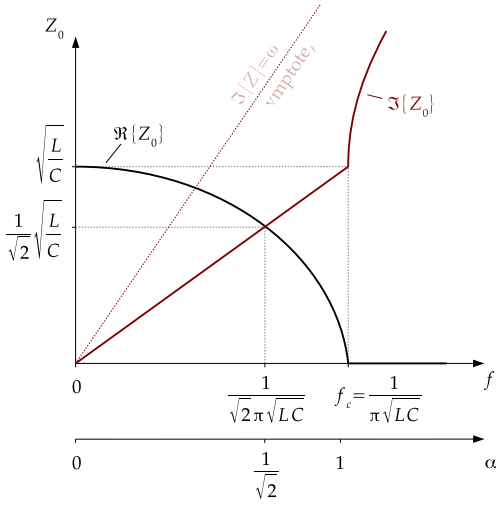


Figure 2.4: Plots of the real and imaginary parts of the characteristic impedance of an LC ladder.

(2.2), and the characteristic impedance for this frequency range is then given by

$$Z_0 = \sqrt{1-\alpha^2}\sqrt{\frac{L}{C}} + j\alpha\sqrt{\frac{L}{C}}. \tag{2.5}$$

Only at DC, the ladder's characteristic impedance is purely real and equal to the well-known expression

$$Z_0 = \sqrt{\frac{L}{C}}. \tag{2.6}$$

The imaginary part of (2.5) increases linearly with frequency, while the real part decreases along a circular arc. For frequencies above the cut-off frequency ($\alpha \geq 1$), the term under the root in (2.2) is positive and the characteristic impedance (plus sign) is purely imaginary and given by

$$Z_0 = j\left(\alpha + \sqrt{\alpha^2-1}\right)\sqrt{\frac{L}{C}}. \tag{2.7}$$

Figure 2.4 plots the real and imaginary parts of the characteristic impedance of the LC ladder as a function of the frequency. It is obvious that the LC ladder's behavior starts to deviate from that of the continuous transmission line at frequencies far below the ladder's cut-off frequency. At $f_c/\sqrt{2}$, the imaginary part of the characteristic impedance is already equal to the real part. Above the cut-off frequency, the impedance converges to the impedance of the input inductor, $j\omega L$, indicated by the asymptote in Figure 2.4.

We usually do not deal with infinite ladder networks, however. A finite length LC ladder is typically terminated in a resistance equal to the ladder's characteristic impedance at DC, given in (2.6). The input impedance of the finite ladder will thus be different

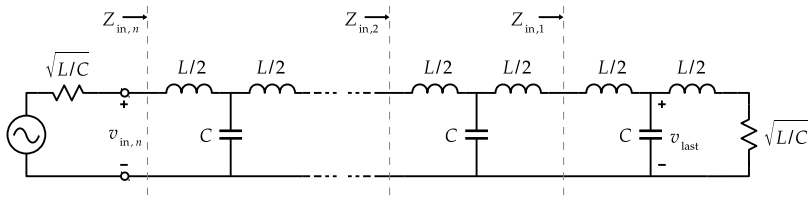


Figure 2.5: Finite LC ladder network ended in inductor half-sections, terminated in a resistance equal to the DC value of its characteristic impedance.

from the characteristic impedance given by (2.2). Additionally, there are several ways to end an LC ladder, also affecting the input impedance. Simply ending in an inductor or capacitor is not ideal. A better option is to end the ladder using an inductor or capacitor half-section, yielding a better bandwidth. An even better, but more elaborate, option is to employ so-called *m*-derived half-sections [Lee04a].

Let's have a look at the input impedance of a finite LC ladder ended in an inductor half-section, as shown in Figure 2.5. Ending the input-end of the LC ladder in a half-size inductor reduces the imaginary part of the input impedance of an LC ladder as (2.5) becomes purely real for frequencies below the cut-off frequency:

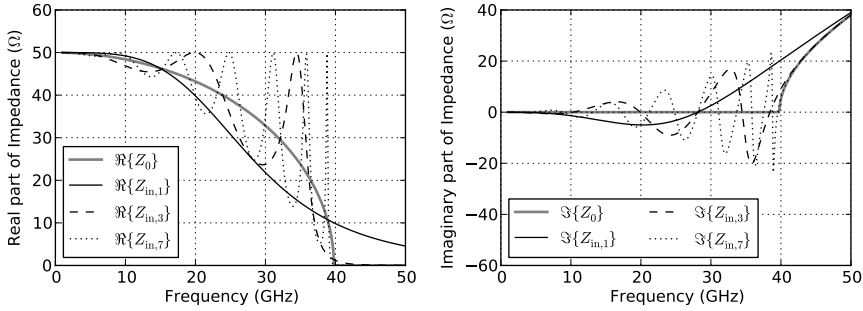
$$\Im\{Z_0\} - \omega\frac{L}{2} = \alpha\sqrt{\frac{L}{C}} - \omega\frac{L}{2} = \frac{\omega\sqrt{LC}}{2}\sqrt{\frac{L}{C}} - \omega\frac{L}{2} = 0. \tag{2.8}$$

This does a great deal to improve the input match of the distributed amplifier. Figure 2.6 shows the input impedance of three LC ladders of different length: one, three and seven sections. The characteristic impedance is plotted in gray for comparison. For increasing number of sections, the input impedance varies wildly with frequency, especially near the cut-off frequency f_c (here around 40 GHz). If the ladder were not ended in the inductor half-section, but just with the capacitor C of the last section, the peaks in the real part of the input impedance would even go all the way up to twice the impedance at DC.

In a practical circuit, losses dampen the peaks somewhat, bringing the input impedance graphs closer to that of the characteristic impedance. The input impedance for LC ladders with the same number of sections as in Figure 2.6, but with a series inductor loss of 1 Ω is shown in Figure 2.7. With or without losses, it is clear that the LC ladder's characteristic impedance starts to deviate significantly from that of the transmission line it approximates already at around half the cut-off frequency.

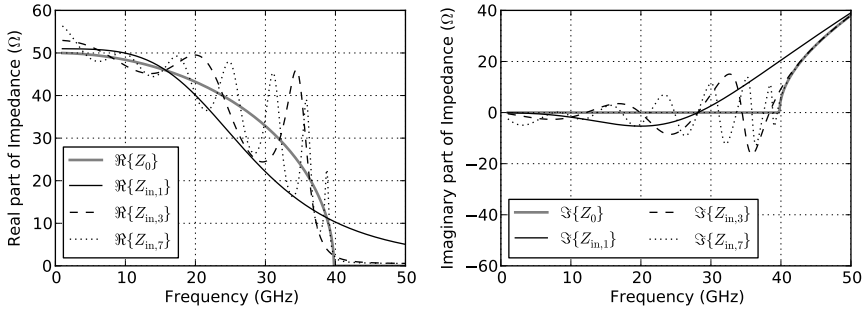
2.1.1.2 Frequency Response

The frequency response of the distributed amplifier is directly determined by the frequency response of the input and output LC ladders. Each input LC ladder section basically looks like the circuit in Figure 2.8. The inductor L forms an LC filter with the MOSFET's gate-source capacitance C, loaded with the input impedance Z_{next} (assumed



(a) (b)

Figure 2.6: (a) Real, and (b) imaginary parts of the input impedance of a finite LC ladder with $L = 400$ pH and $C = 160$ fF of 1, 3 and 7 ladder sections compared to the characteristic impedance. The cut-off frequency of the ladder is 39.8 GHz.



(a) (b)

Figure 2.7: (a) Real, and (b) imaginary parts of the input impedance of the finite LC ladder of Figure 2.6, but this time with a series loss of 1 Ω in the inductors.

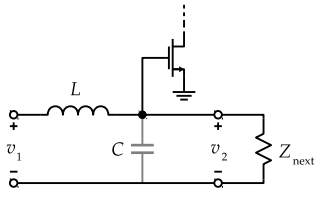


Figure 2.8: A single section of an LC-ladder based distributed amplifier is basically a loaded LC filter.

real) of the next section. The transfer function of this filter is given by

$$G(s) = \frac{v_2}{v_1} = \frac{1}{1 + s\frac{L}{Z_{\text{next}}} + s^2 LC} = \frac{1}{1 + j\omega\frac{2\zeta}{\omega_n} + \left(\frac{j\omega}{\omega_n}\right)^2}. \tag{2.9}$$

The damping ratio of this filter is given by

$$\zeta = \frac{1}{2}\sqrt{\frac{L}{C}}\frac{1}{Z_{\text{next}}}. \tag{2.10}$$

When we approximate Z_{next} with the characteristic impedance at DC $\sqrt{L/C}$, the damping ratio equals $\frac{1}{2}$; the response is slightly underdamped, resulting in very slight peaking in the frequency domain [Dor01]. The flat frequency response is a typical characteristic of the distributed amplifier, allowing for broadband operation. The natural frequency,

$$f_n = \frac{\omega_n}{2\pi} = \frac{1}{2\pi\sqrt{LC}} \tag{2.11}$$

is where the transfer function dips below unity. It is exactly one half of the cut-off frequency f_c of the infinite LC ladder.

Of course, in a distributed amplifier, several LC sections are cascaded to form the ladder. The load impedance for each section Z_{next} is equal to the input impedance of the next section, altering the frequency response. Similar to the plots of the characteristic impedance, Figure 2.9 shows the voltage gain for LC ladders of 1, 3 and 7 sections. The voltage gain is defined in terms of the voltages indicated in Figure 2.5:

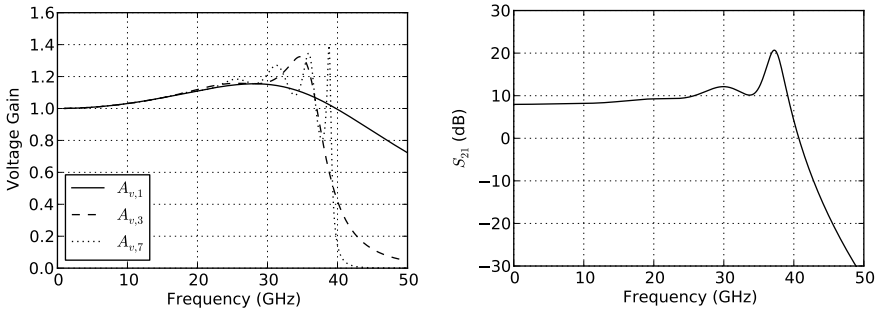
$$A_{v,n} = \frac{v_{\text{last}}}{v_{\text{in},n}}, \tag{2.12}$$

modeling the transfer function of the input signal of the amplifier to the input signal to the right-most gain cell. It is interesting to see that the bandwidth of the ladder is close to its cut-off frequency, double of the LC-filter's natural frequency. However, the response is still fairly flat overall, except near the cut-off frequency, where the peaking can help to compensate for skin-effect losses that increase with frequency.

In a distributed amplifier, the signals on both the input and output LC ladders are subjected to the ladder transfer function. Figure 2.9b shows the gain of a lossless four-section distributed amplifier employing the same inductors and capacitors used in the previous plots and a 25 mS gain cells. The gain shows a similar, but more pronounced peaking near the cut-off frequency due to the added peaking of the output LC ladder.

2.1.2 Transmission Lines

Instead of building LC ladders using the transistors' parasitic capacitances, actual transmission lines can be used. Candidates for use in monolithic integrated distributed amplifiers are microstrip lines and coplanar waveguides (CPW). Identical transistors plug in to the transmission line at regular intervals, forming a *capacitively-loaded transmission line* [Col01]. A representation of such a line is shown in Figure 2.10,



(a) (b)

Figure 2.9: Voltage gain of (a) the LC ladder of 1, 3 and 7 ladder sections, and (b) forward gain of a four-section distributed amplifier built using the same LC ladder section ($g_m = 25$ mS and $Z_0 = 50\ \Omega$).

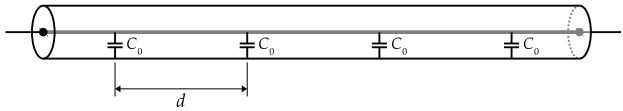


Figure 2.10: A capacitively loaded coaxial transmission line.

in which a coaxial transmission line has lumped capacitors C_0 connected in shunt at intervals d. The periodicity introduced by these capacitors brings about a stop-band in the frequency response of the line. The frequency response of a periodic structure shows alternating pass- and stop-bands[2]. The location of the first stop-band determines the bandwidth of the distributed amplifier.

Adding extra capacitance to a transmission line also alters its characteristic impedance. A transmission line is typically modeled by per-unit-length resistance, inductance, conductance and capacitance (RLGC) parameters, and represented by the equivalent circuit shown in Figure 2.11. The characteristic impedance of a lossless line ($R = 0$, $G = 0$) is given by [Col01]

$$Z_0 = \sqrt{\frac{L}{C}} \tag{2.13}$$

[2]Periodic structures are also used as slow-wave structures, showing a phase velocity much less than that of light.

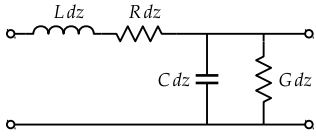


Figure 2.11: Equivalent circuit of an infinitesimal transmission line section.

Referring again to Figure 2.10, the lumped capacitances C_0 increase the average per-unit-capacitance of the line to

$$C' = C + \frac{C_0}{d}, \tag{2.14}$$

lowering the characteristic impedance to

$$Z_0' = \sqrt{\frac{L}{C + \frac{C_0}{d}}}. \tag{2.15}$$

To obtain a distributed amplifier with a 50 Ω input transmission line, the characteristic impedance of the input transmission line before attaching the transistors should thus be higher than 50 Ω. However, it is not easy to produce transmission lines with a high characteristic impedance in integrated circuits, and especially in standard CMOS technology, due to the required dimensions of the lines. A practical limit of what is achievable lies around 100 Ω.

Take, for example, a CPW implemented using the top metal layer in a 90 nm RF-CMOS process. At 50 GHz, its per-unit-length parameters are $R = 6$ Ω/mm, $L = 545$ pH/mm, $G = 0.5$ mS/mm and $C = 72$ fF/mm. Employing (2.13), its characteristic impedance is determined to be 87 Ω. To obtain a net characteristic impedance of 50 Ω, the spacing between transistors with a gate capacitance of 25 fF[3] needs to be

$$d = \frac{C_0}{C}\frac{Z_0'^2}{Z_0^2 - Z_0'^2} = \frac{25\text{ fF}}{72\text{ fF/mm}}\frac{50^2}{87^2 - 50^2} = 0.17\text{ mm}, \tag{2.16}$$

as can be readily derived from (2.15) and (2.13).

As with the LC ladder, the periodically loaded line's behavior starts to deviate from that of a continuous transmission line for high frequencies. For frequencies where the wavelength is large with respect to the interval d, the line will appear smooth, however. Figure 2.12 shows the characteristic impedance of our CPW, periodically loaded with 25 fF capacitors. Spacing the capacitors 0.17 mm apart indeed yields a line with a characteristic impedance of 50 Ω.

Only at 150 GHz the characteristic impedance starts to drop appreciably. This roughly marks the location of the stop-band, which is determined by the capacitor's size relative to the transmission line's per-unit-length capacitance and the interval d. To illustrate the existence of multiple stop-bands, Figure 2.13 shows the propagation constant of the same capacitively loaded CPW, but this time with an interval of 1 mm, shifting the first two stop-bands to frequencies below 200 GHz. The stop-bands are apparent in the attenuation constant plot (Figure 2.13a), where ranges of increased attenuation appear. The stop-bands are also clearly visible in the characteristic impedance plot (Figure 2.14); the real part is close to zero and the imaginary part is large. More information about periodic structures can be found in literature [Col01].

Figure 2.15 shows the gain and input impedance of a six-section distributed amplifier employing the CPW discussed above and 20 mS gain cells with 20 fF input and output

[3] From the unity-gain frequency f_T characterizing this 90 nm technology, the maximum transconductance gain of an NMOS transistor with a 25 fF gate capacitance is about 20 mS.

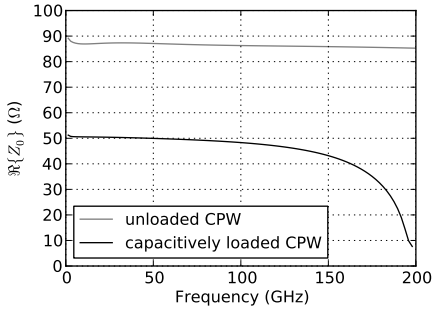
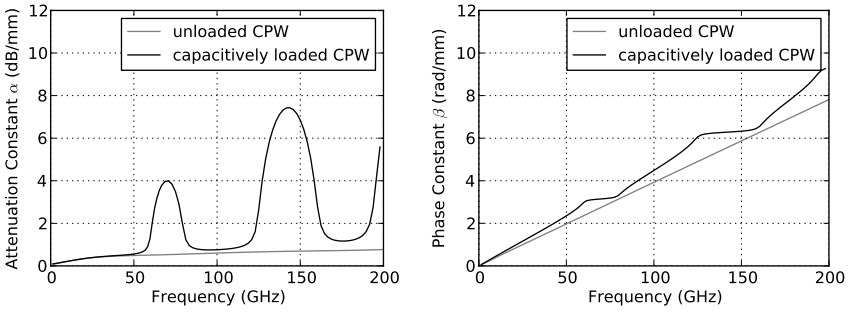
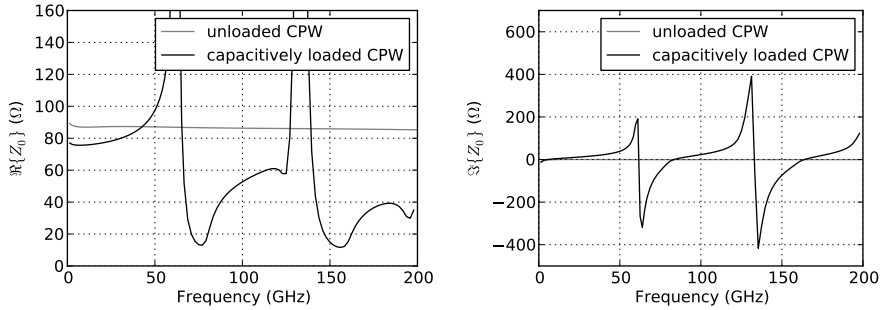


Figure 2.12: Real part of the characteristic impedance of the capacitively loaded line with an interval of 0.17 mm as a function of frequency. The characteristic impedance of the unloaded CPW is shown in gray.



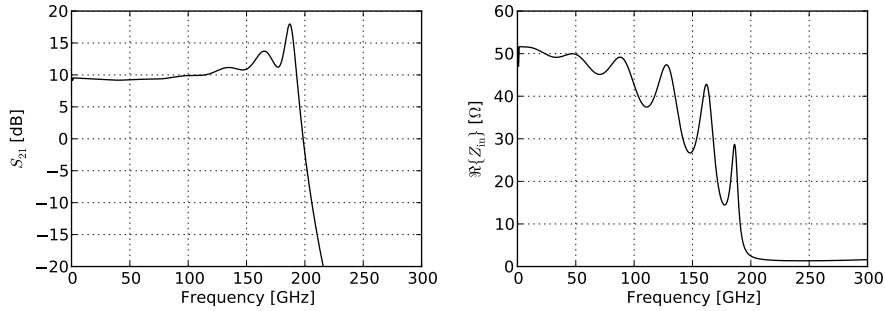
(a) (b)

Figure 2.13: Propagation constant of the capacitively loaded CPW with an interval of 1 mm: (a) attenuation constant, and (b) phase constant. The propagation constant for the unloaded CPW is shown in gray.



(a) (b)

Figure 2.14: Characteristic impedance of the capacitively loaded CPW with an interval of 1 mm: (a) real part, and (b) imaginary part. The characteristic impedance for the unloaded CPW is shown in gray.



(a) (b)

Figure 2.15: (a) Gain, and (b) real part of the input impedance of a six-section CPW-based distributed amplifier with 20 mS gain cells.

capacitance. The gain response shows peaking near the cut-off frequency similar to that of an LC-ladder based distributed amplifier. Also the frequency-dependence of the input impedance is similar to that of the LC ladder. Note that the capacitively loaded CPW has been ended, as in the LC-ladder implementation, using CPW sections of half length. Their effect corresponds to that of the inductor half-sections in LC ladders.

As the parasitic capacitance of planar spiral inductors becomes increasingly problematic at high frequencies, transmission line-based distributed amplifiers are better suited for achieving very large bandwidths[4]. On the downside, the characteristic impedance of transmission lines in integrated circuits is limited. This requires gain cells to be spaced relatively large apart, requiring a large die area.

[4]The threshold lies around 40 GHz for fully integrated distributed amplifiers.

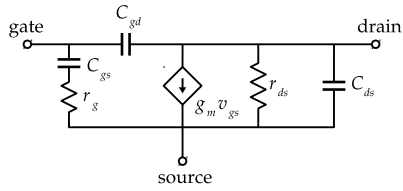


Figure 2.16: Intrinsic small-signal model of a MOS transistor, where losses are represented by the drain-source and non-quasi-static gate resistances, r_{ds} and r_g respectively.

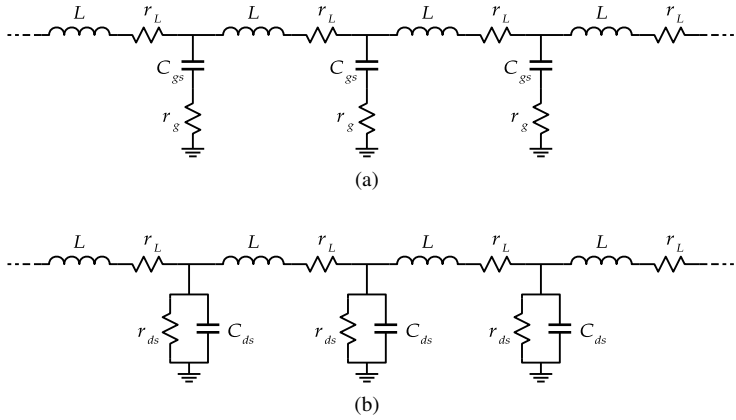


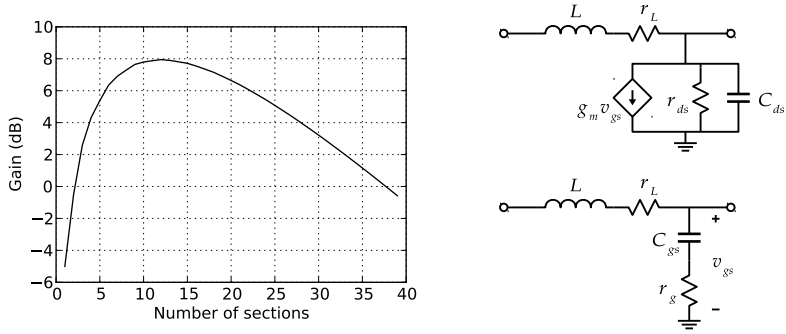
Figure 2.17: (a) Lossy input, and (b) output LC ladders.

2.2 Losses and Other Non-Idealities

In the absence of losses, the number of cells in a distributed amplifier could be increased indefinitely, allowing any gain to be obtained. Losses in the input and output transmission lines attenuate the input and output signals respectively, and limit the number of cells in a practical distributed amplifier. Additionally, the transistors also introduce losses. These are represented in the MOSFET small-signal model by the non-quasi static gate resistance[5] r_g and the drain-source resistance r_{ds}, shown in Figure 2.16. The resistivity of the poly-silicon gate is not considered here.

Taking these losses into account, but ignoring the gate-drain capacitance for now, the input and output LC ladders take the form shown in Figures 2.17a and 2.17b respectively. The input signal traveling down the lossy input ladder is attenuated, therefore exciting each transistor with a lower voltage than the previous one. Similarly, the output line attenuates the transistor output currents. Whereas the transistor closest to the input is excited with the largest voltage, its output signal has to travel the farthest to the output terminal and is attenuated most.

[5]The non-quasi static gate resistance models the delay in the channel charge buildup in the FET and is equal to $\frac{1}{5g_m}$ [Tsi99, Jan01].



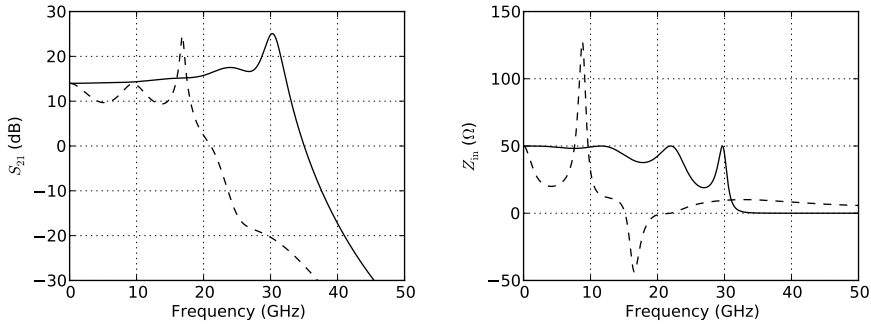
(a) (b)

Figure 2.18: (a) Gain versus number of distributed amplifier sections with (b) a unit section with $L = 400$ pH, $C_{gs} = C_{ds} = 160$ fF, $r_L = 5\ \Omega$, $r_g = 10\ \Omega$, $r_{ds} = 500\ \Omega$ and $g_m = 20$ mS.

Up to a given number of sections, the gain of the distributed amplifier increases with each section added, benefiting from the gain-delay trade-off typical of the distributed amplifier. At a certain point however, the gain contributed by an additional section (additive) cannot compensate for the extra losses introduced by the longer LC ladders (multiplicative). To illustrate this, Figure 2.18a shows the gain of a distributed amplifier as a function of the number of sections. Figure 2.18b depicts the section model used in this distributed amplifier. Initially, the gain increases steadily with the number of sections up to a maximum gain of 8 dB for 12 sections. When further increasing the number of sectionss, the total loss in the lines becomes too large and the gain starts to drop.

While Figure 2.18a clearly illustrates the limitations imposed by the losses present in a distributed amplifier, the problem is more complex than this as losses on the input and output lines also affect the frequency response of the amplifier through RC filtering [Bey84]. It should also be noted that the losses, and in particular the losses due to skin effect in the series inductors or transmission lines, are frequency-dependent. This leads to losses increasing with frequency, disturbing the flat frequency response of the distributed amplifier. The underdamped response of the distributed amplifier and the associated slight frequency peaking can help compensate for this. If this is not sufficient, extra measures need to be taken to increase the gain at the high end of the frequency band.

Previously skipped in the discussion, the gate-drain capacitance C_{gd} of a MOSFET also affects the operation of the distributed amplifier. This capacitance feeds back a portion of the output signal to the input line, possibly leading to instabilities. Often, cascode gain cells are used to improve reverse isolation. Figure 2.19a shows the effect of the feedback capacitor C_{gd} on the operation of the amplifier. Miller multiplication of C_{gd} significantly increases the input capacitance of the MOSFET [Raz01], and thus changes the characteristic impedance and bandwidth of the LC ladder. It should therefore be



(a) (b)

Figure 2.19: (a) Gain and (b) real part of the input impedance of a (lossless) four-section transmission-line based distributed amplifier without (solid line) and with (dashed line) the feedback capacitor C_{gd}.

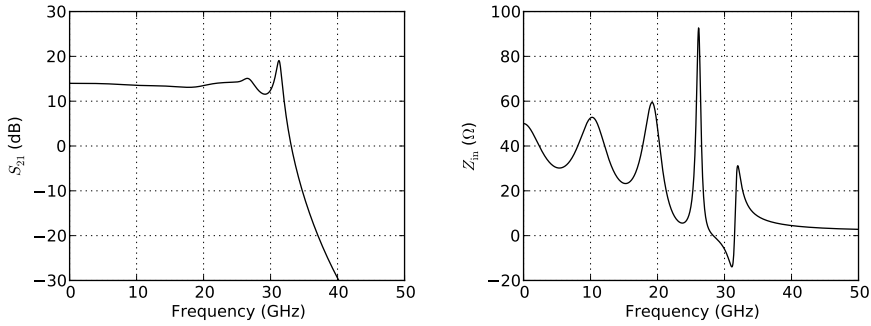
taken into account at the start of the design of a distributed amplifier. The capacitance can also lead to instabilities, reflected by the negative input impedance in Figure 2.19b. Making use of cascode gain cells, shown in Figure 2.20, the impact of C_{gd} can be reduced at the cost of an increased power consumption. However, the presence of the large capacitance at the internal cascode node introduces a non-dominant pole which can also affect the bandwidth of the amplifier. Some authors apply inductive peaking to mitigate the effect of this pole on the transfer function [Hey07, Chi07], but the extra inductors add to the complexity of the circuit and the amount of die area required.

On a positive note, the feedback-effect provided by C_{gd} can also be exploited to peak the frequency response, compensating for skin-effect losses [Koh68]. Furthermore, C_{gd} can give rise to a mythical *exponentially growing wave*, which received a lot of attention from researchers in the past and is the subject of Chapter 5.

Finally, in distributed power amplifiers, breakdown can be an issue. The distributed amplifier is a good choice for high-power applications, since it is in fact a parallel power combiner, allowing to output a higher signal power than a cascade amplifier. However, the gain cell currents add in the output transmission line and can increase the voltage on the gain cell outputs to the point where breakdown can occur. Nevertheless, the distributed amplifier has an advantage over cascade amplifiers with respect to breakdown, as only part of the current flows through a single gain cell, which makes hot carrier degradation less likely to occur [Aok08].

2.3 Properties of the Distributed Amplifier

In this section, we look at the secondary properties of an amplifier: noise and distortion. In a first subsection, the sources of noise and the propagation of the noise power to the output of the distributed amplifier are discussed. The second subsection briefly covers the linearity of the distributed amplifier. Both discussions also make the comparison



(a) (b)

Figure 2.20: (a) Gain and (b) real part of the input impedance of the four-section distributed amplifier employing cascode gain cells (with feedback capacitor C_{gd}).

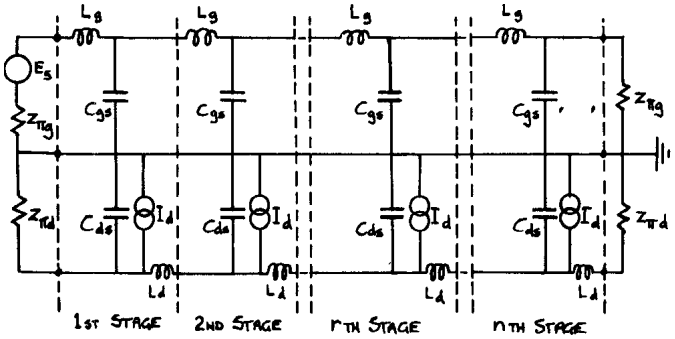


Figure 2.21: The distributed amplifier model used by Aitchison for noise analysis [Ait85].

with the conventional cascade amplifier.

2.3.1 Noise

There are two groups of noise sources in the distributed amplifier; noise associated with the transistors and thermal noise due to the termination resistors and losses. In the case of field effect transistors, the noise generated by the transistors includes the channel thermal noise, gate-induced noise and flicker noise. The former two are correlated, rendering noise analysis all the more challenging. Flicker noise, also called $1/f$ noise, is only significant at frequencies below the *corner frequency*, typically in the vicinity of 1 MHz for submicron transistors [Raz01] and can be ignored in distributed amplifiers.

Aitchison calculated the intrinsic noise figure of the MESFET distributed amplifier in 1985, assuming loss-free and unilateral MESFETs and lossless inductors, as shown in Figure 2.21 [Ait85]. In addition, the per-section delay of the input and output LC

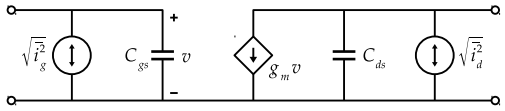


Figure 2.22: The FET model used by Aitchison, including equivalent gate $\left(\sqrt{\bar{i}_g^2}\right)$ and drain $\left(\sqrt{\bar{i}_d^2}\right)$ noise generators.

ladders $\beta_g = \beta_d = \beta$ is assumed to be equal. To calculate the noise figure, the available noise power at the output of the amplifier due to each noise source is determined.

The contribution of the source impedance is equal to its available noise power kT_0B [Lee04a] times the forward available power gain of the amplifier

$$G_f = \frac{N^2 g_m^2 Z_{\pi g} Z_{\pi d}}{4}, \tag{2.17}$$

where N is the number of stages and $Z_{\pi g}$ and $Z_{\pi d}$ are the characteristic impedances of the input (gate) and output (drain) LC ladders, respectively (also refer to Figure 2.21). Similarly, the contribution of the input LC ladder's termination resistance is equal to

$$G_r kT_0 B. \tag{2.18}$$

where G_r is the reverse available gain, given by

$$G_r = \frac{g_m^2 Z_{\pi g} Z_{\pi d}}{4} \left(\frac{\sin N\beta}{\sin \beta}\right)^2. \tag{2.19}$$

Finally, the noise generated by the left-hand drain line termination resistor simply travels down the (loss-free) drain line and its available power thus equals kT_0B.

The noise generated in the MESFETs is represented by gate and drain current sources (Figure 2.22), together with a coefficient $c = j0.395$ that expresses the correlation between them [vdZ62, vdZ63]. The noise contribution from each of these noise current sources, for all transistors in the distributed amplifier, is calculated. Since both the gate and drain noise current sources feed purely real impedances, and the correlation coefficient is purely imaginary, there is no correlation contribution to the power dissipated in the load. The total noise power dissipated in the load can be, surprisingly, reduced to a concise equation. Summing all contributions, an expression for the noise factor F of the distributed amplifier is obtained:

$$F = 1 + \left(\frac{\sin N\beta}{N \sin \beta}\right)^2 + \frac{4}{N^2 g_m^2 Z_{\pi g} Z_{\pi d}} + \frac{Z_{\pi g} \omega^2 C_{gs}^2 R \sum_{r=1}^{N} f(r,\beta)}{N^2 g_m} + \frac{4P}{N g_m Z_{\pi g}} \tag{2.20}$$

with

$$f(r,\beta) = (N - r + 1)^2 + \left(\frac{\sin(r-1)\beta}{\sin \beta}\right) + \frac{2(N-r+1)\sin(r-1)\beta \cos r\beta}{\sin \beta}. \tag{2.21}$$

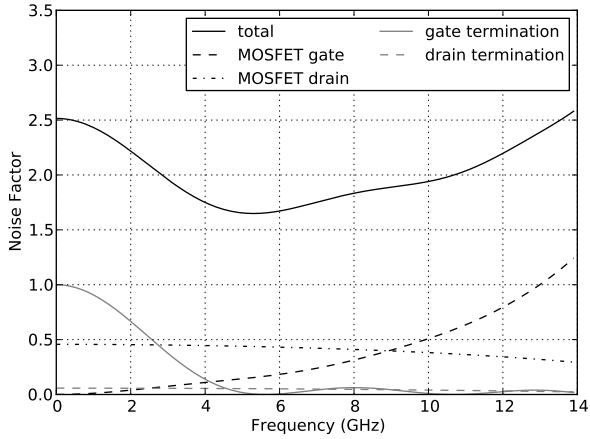


Figure 2.23: Breakdown of the various contributions to the noise factor in a 5-section distributed amplifier.

In these expressions, P and R are FET noise parameters. The first three terms in (2.20) correspond to the noise generated by the source impedance, the input termination resistor and the left-hand drain termination resistor. The last two terms are due to the transistor gate and drain noise sources, respectively.

The first term due to the source impedance, 1, is equal for all amplifier topologies. The second term has peaks with a maximum of 1 when β is an integer multiple of π, but otherwise decreases with the number of gain cells N. Also, the peaks become narrower for larger N. The third and fifth terms are inversely proportional to N^2 and N respectively. The fourth term turns out to be, after some simplification trickery on $f(r,\beta)$, proportional to N. Thus, there exists an optimum value of N, minimizing the noise figure. Calculating this optimum noise figure, Aitchison concludes that the optimal noise performance of the distributed amplifier is similar to that of a resonant amplifier.

It is interesting to visualize the different noise contributions to the noise factor. Figure 2.23 shows the relative values of the terms in (2.20) for the 5-section noise-optimized distributed amplifier described by Aitchison. It is immediately obvious that the noise from the left-hand drain termination resistor, since it is not amplified by the transistors, is negligible. The noise factor due to the gate line termination resistor shows the distinct $\frac{\sin N\beta}{N\sin\beta}$ shape. It is the largest contributor at low frequencies, but is negligible elsewhere. The second peak of the $\frac{\sin N\beta}{N\sin\beta}$ curve always lies beyond the cut-off frequency of the LC ladder, and thus should not be considered. Above 3 GHz, the noise generated by the transistors is dominant, with the gate-induced noise increasing steeply at the high end of the band.

According to Heydari [Hey07], the noise analysis made by Aitchison suffers from an analytical misconception; namely it assumes that the magnitude square of the Fourier transform of the total noise current is equal to the PSD (power spectral density) of the

noise current. This is false since the Fourier transform of a random process does not carry useful insight, as it is a random process by itself. Also, Aitchison ignores the partial correlation between the gate-induced and thermal noise sources. Correcting these shortcomings of Aitchison's analysis, Heydari obtains an expression for the noise factor:

$$F_{\text{tot}} = 1 + F_{\text{flicker}} + \frac{1}{(Ng_mZ_T)^2} + \left(\frac{\sin N\beta}{N\sin\beta}\right)^2 + \frac{\gamma}{Ng_mZ_T} \times \left[1 + \frac{2\left(N^2+1\right)}{3}\left|\frac{\kappa_c}{c}\right|^2(\omega\tau_{GS})^2 + 2N\kappa_c\omega\tau_{GS}\right] \tag{2.22}$$

where $Z_T = Z_G = Z_D$, the characteristic impedance of the gate and drain lines[6], $\kappa_c = |c|\sqrt{\frac{\delta\zeta}{\gamma}}$ and τ_{GS} models the frequency response of the cascode gain cells. Heydari also calculates the FET flicker noise contribution F_{flicker}; a valiant effort but rather pointless, illustrated by the sub-1 MHz corner frequency for the presented amplifier.

Expressing the R and P noise parameters [BT80] used by Aitchison in terms of the now more commonly used parameters γ, δ and ζ [Goo02]

$$R = \delta\zeta \tag{2.23}$$
$$P = \gamma, \tag{2.24}$$

we can compare the expressions for the noise factor obtained by Aitchison (2.20) and Heydari (2.22). As the analysis made by Heydari only differs with respect to the MOSFET noise sources, the terms due to the other noise sources should be equal. Whereas the term corresponding to the gate line termination resistor thermal noise are the same in (2.20) and (2.22), the term due to the drain line termination resistor differs by a factor of four. This difference stems from Heydari's incorrect use of the total noise power instead of the available noise power in calculating the noise at the output of the amplifier due to the source impedance and the gate termination resistor. This error in the calculation of the latter also results in a factor-of-four error of the FET's contribution to the noise figure. Correcting these, only the term in (2.20) corresponding to the gate noise current generator is different in (2.22). The output noise due to the latter is very high after correcting these (Figure 2.24), even much higher than the measured noise of the prototype amplifier presented in the paper. These and some other inconsistencies in the article unfortunately render it useless.

Both the analyses by Aitchison and Heydari above do not take into account the losses present in the inductors and transistors. Ko and Kwon performed a similar noise analysis as Aitchison, but including losses and the correlation between the noise current sources in the FET [Ko05]. The losses introduce another term in the noise factor expression that increases with the number of sections, leading to a significantly higher noise figure at high frequencies, and thus should be taken into account in broadband LNA design.

[6] Z_G and Z_D correspond to $Z_{\pi g}$ and $Z_{\pi d}$, respectively.

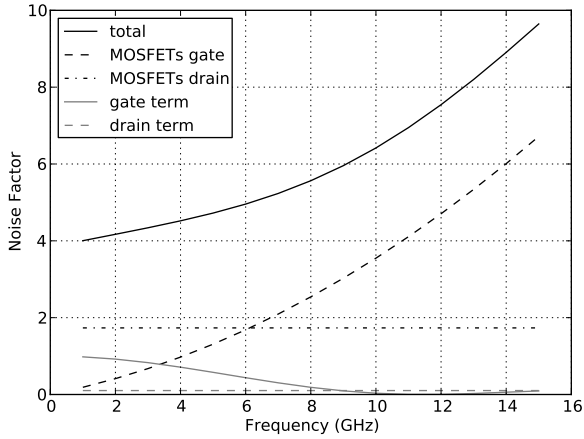


Figure 2.24: Breakdown of the various contributions to the noise factor in the 3-section distributed amplifier presented by Heydari [Hey07].

2.3.2 Distortion

Contrary to noise analysis, distortion analysis of the distributed amplifier is more straightforward. Being the only non-linear components in the distributed amplifier, the transistors fully determine its linearity performance. The harmonic and intermodulation distortion signals from the different transistors add in phase just like the signals at the fundamental frequency. Any theory relating to the distortion of the employed gain cells (common source, cascode) is thus directly applicable to the distributed amplifier. For example, MOSFETs can be biased at the so-called "sweet spot" in moderate inversion, where there is a peak in the third-order intercept point [Too04].

The distributed amplifier has an important advantage when compared to conventional cascade amplifiers; for a constant output power, the third-order intermodulation distortion decreases with the number of sections. Adding an extra section to a distributed amplifier increases its gain, allowing the input power to reduce for the same output power. This reduction in input power reduces the intermodulation products in each of the transistors, and thus also the distortion of the output signal. Compare this to the conventional cascade amplifier, where an extra stage also allows a reduction of the input signal, reducing the distortion in the first stage. However, in contrast with the distributed amplifier, the intermodulation product of the first stage is amplified in subsequent stages, on top of adding their own intermodulation products [Lee04a].

Only considering the main contribution to distortion in MOSFETS, the nonlinear transconductance, the small-signal output current of a non-linear FET is given by the power series

$$i_d = g_{m1} v_{gs} + g_{m2} v_{gs}^2 + g_{m3} v_{gs}^3 \tag{2.25}$$

where v_{gs} is the gate-source voltage and g_{m1}, g_{m2} and g_{m3} model the non-linear transconductance. The ratio of the output power at the fundamental frequency to the third-

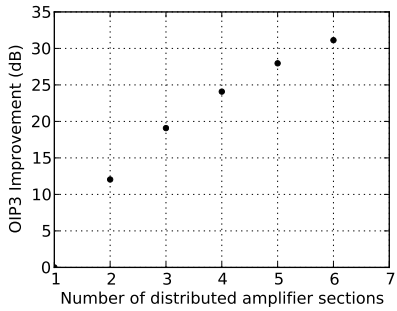


Figure 2.25: Output-referred third-order intercept improvement as a function of the number of distributed amplifier sections with respect to a single-section amplifier.

order intermodulation product for an N-section lossless distributed amplifier is given by [Ait01]

$$\mathrm{OIP3} = \left(\frac{g_{m1}^3}{3 \cdot i_{\mathrm{tot}} \cdot g_{m3}} \right)^2 \cdot N^4 \tag{2.26}$$

where i_{tot} is the total output current at the fundamental frequency and N is the number of distributed amplifier sections. The fourth power suggests a large improvement of the linearity performance with the number of sections. The improvement of the output-referred third order intercept versus the number of stages is shown in Figure 2.25, with $N = 1$ section as the reference.

2.4 Variations on the Distributed Amplifier

In this section some variations on the distributed amplifier topology are discussed together with their advantages and disadvantages.

2.4.1 Cascaded Single-stage Distributed Amplifier

Figure 2.26 shows a three-stage cascaded single-stage distributed amplifier (CSSDA), a cascaded amplifier in which the stages are single-stage distributed amplifiers [Ban00]. In all but the first and last stages, the left half of the output transmission line is omitted and all of the stage's output current contributes to the gain. As the characteristic impedance of the interstage transmission lines do not depend on the source or the load, it can be increased, boosting the gain. The voltage gain of the CSSDA is given by

$$A_v = \frac{1}{2} g_m^N Z_{0\mathrm{int}}^{N-1} Z_0. \tag{2.27}$$

Comparing (2.27) to (2.1), it is obvious that the gain provided by a CSSDA can be much higher than that of a classic distributed amplifier.

The first and last stage of a CSSDA provide a good broadband input and output match, typical of distributed amplifiers. Cascading of the stages and the optimization of the

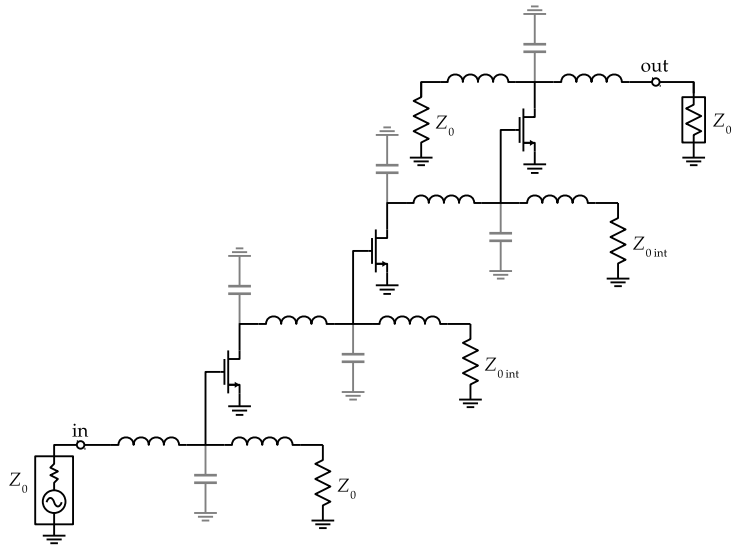


Figure 2.26: A three-stage cascaded single-stage distributed amplifier.

interstage characteristic impedance allows for a high gain. There are also some downsides to the CSSDA, though. The topology is less suited for high-power applications, as the total output power is limited by the last stage, whereas the classic distributed amplifier benefits from its power combining ability. Elimination of half of the interstage transmission lines is also not without consequence. The transistor is now at the end of the LC ladder, affecting the properties of the ladder (see Section 2.1.1). In fact, the interstage network, as described by Banyamin, is not an LC ladder approximating a transmission line but a matching network. The "characteristic impedance" $Z_{0\mathrm{int}}$ has a large imaginary part and shows a strong frequency dependence, used to compensate for the negative gain roll off of the transistors. For these reasons, it is perhaps not correct to label the CSSDA as a distributed amplifier, as the two do not show many similarities, even though it seems that way at first sight. It also suggests that the CSSDA topology might not be suited for very broadband amplifiers.

2.4.2 Matrix Amplifier

In the matrix amplifier, several distributed amplifiers are cascaded in a matrix structure; instead of simply connecting the individual amplifiers in series, the individual distributed amplifiers are stacked, sharing a single transmission line [Nic87]. Note that the signal delays between the inputs and the outputs of the parallel gain cells should still match as in a classic distributed amplifier (see Section 2.1). An example of a 2×3 matrix amplifier is shown in Figure 2.27.

The matrix amplifier solves an important problem with cascaded distributed amplifiers; it eliminates a lot of the loss associated with the long interstage transmission line. However, it also introduces a new problem. As the output currents of each gain cell

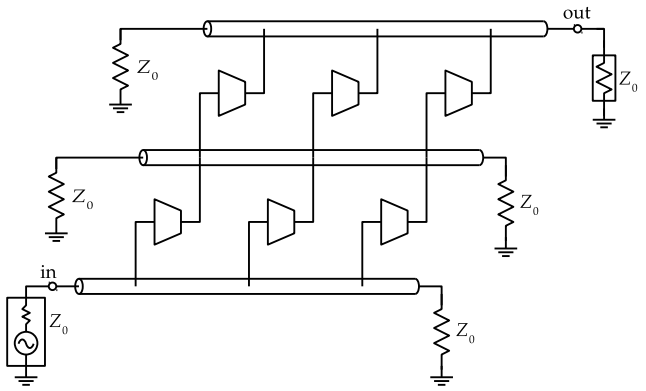


Figure 2.27: A 2×3 matrix amplifier consists of a stacked cascade of two three-section distributed amplifiers.

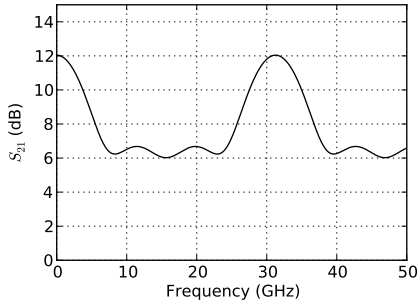


Figure 2.28: Distinctive non-flat gain of a matrix amplifier.

in a distributed amplifier split into forward and reverse parts, the voltage at any point on the output transmission line is the superposition of a forward and a reverse wave. The reverse waves add incoherently (see Section 2.1), and are therefore a useless byproduct of distributed amplification. In the classic distributed amplifier, these are safely discarded in a termination resistor. In the matrix amplifier on the other hand, these reverse waves are also being amplified by the second-stage gain cells, leading to a strongly frequency-dependent gain. For illustration, Figure 2.28 shows the gain of an ideal 2×4 matrix amplifier employing lossless transmission lines and 20 mS gain cells (no lumped capacitances). The amplifier has a gain variation of 6 dB. It is easy to recognize the $\frac{\sin nx}{\sin x}$ shape of the reverse gain that we encountered in the noise analysis of the distributed amplifier.

The gain flatness of a matrix amplifier can be improved by tinkering with the interstage transmission lines. Doubling two of the inductances in the center LC ladder in the above-mentioned 2×4 amplifier, the gain variation can be reduced to 4 dB, at the same time increasing the average gain. Increasing the inductances changes the delay (and characteristic impedance) of the corresponding sections, thus altering the way the currents from the gain cells interact. The gain can be further flattened by taking

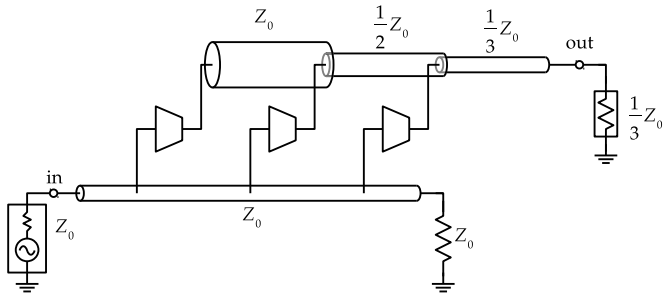


Figure 2.29: A three-section tapered distributed amplifier.

this approach a couple of steps further: subjecting all amplifier elements to individual optimization, adding input and output matching networks and inserting series inductive elements at the drain terminals of the transistors. Niclas' measurements of an experimental realization of the optimized 2×4 amplifier show a fairly flat, 13.8 ± 0.8 dB gain from 2 to 21.5 Ghz and < -10 dB input and output reflection. This performance is comparable to that of an optimized cascade of two 4-transistor distributed amplifiers, but the matrix amplifier occupies a smaller die area and has better noise figure and input matching.

It is admirable to see that it is possible to obtain a flat gain across a wide bandwidth with the help of circuit optimization. While the optimization might lead to a flat gain response, the group delay may show large variations, however. More importantly, the inherent frequency-dependence of the gain makes it extremely difficult to gain insight in the basic operation of a matrix amplifier.

.

2.4.3 Tapered Distributed Amplifier

An unfortunate property of the distributed amplifier is that half of each gain cell's output current is lost in an internal termination resistor, severely limiting the efficiency of the amplifier. In the matrix amplifier discussed above, these reverse waves are also being put to use. However, these lead to a strongly frequency-dependent gain and half of the output current of the transistors in the last stage still goes to waste.

By tapering the output transmission line of a distributed amplifier, it is possible to completely eliminate the reverse waves [Gin48]. In this configuration, all of the output current flows into the load impedance, effectively doubling the amplifier's output current. Figure 2.29 shows a three-stage distributed amplifier with a tapered output transmission line. The relative values of the characteristic impedances of the transmission line sections are chosen such that a gain cell's left-bound current neutralizes the reflected part of the current coming from the left at each intersection. For an N-section distributed amplifier, the characteristic impedances should scale according to $1/k$ where k is the section number, counting from the left[7].

[7] A detailed derivation can be found in Section 3.1

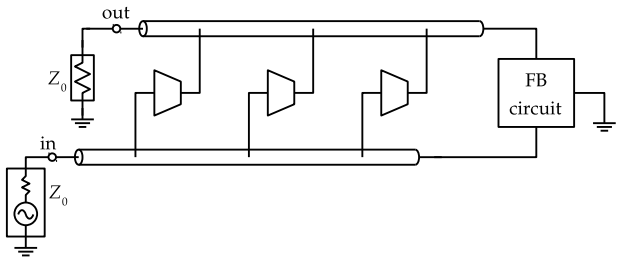


Figure 2.30: A three-section distributed amplifier with internal feedback [Arb08]. The authors do not provide details about the filter circuit in the feedback path.

This seemingly simple adjustment to the distributed amplifier doubles the output current. However, the load impedance needs to be N times lower for reasons that are explained in Chapter 3, so the available output power is not necessarily higher[8] It is also important to note that the tapered distributed amplifier's operation depends on the exact interaction of the reverse currents. When losses are present, the relative magnitudes of these currents are affected, and the reverse currents may not be perfectly canceled, reflecting at the left extremity of the transmission line and giving rise to a frequency-dependent response.

Another point of concern in the use of tapered lines is related to output matching. The output transmission line of a classic distributed amplifier is terminated with its characteristic impedance Z_0 at the left end and thus presents an output impedance of Z_0 across the spectrum. In a tapered distributed amplifier, the output impedance is frequency-dependent as the output transmission line is not terminated on the left. Therefore, it is important that the load impedance matches the characteristic impedance of the last line section, minimizing reflections. In a practical implementation though, losses in the inductors and the output conductances in the gain cells attenuate these reflected signals.

2.4.4 Distributed Amplifier with Internal Feedback

Arbabian and Niknejad presented a distributed amplifier with internal feedback in 2008 [Arb08]. Depicted in Figure 2.30, the amplifier is basically a classic distributed amplifier, but its output signal is fed back to the input transmission line, having it pass through the distributed amplifier a second time. In other words, the amplifier is cascaded with itself! The undesired, frequency-dependent reverse-amplified signal precedes the coherently amplified output signal, introducing some frequency-dependence in the net gain. However, this signal is not amplified twice like the forward-amplifier signal is, and thus is much smaller.

An attempt to analyze the distributed amplifier with internal feedback is troubled by the existence of multiple feedback loops. Luckily, signal flow graph (SFG) theory [Mas53a, Mas56] comes to the rescue, enabling the derivation of the amplifier's transfer function in a straightforward manner. Figure 2.31 depicts a two-section distributed amplifier with internal feedback. The currents i_a to i_n indicated in the figure have been chosen

[8] Chapter 3 presents an alternative tapering scheme that eliminates the need for a lowered load impedance.

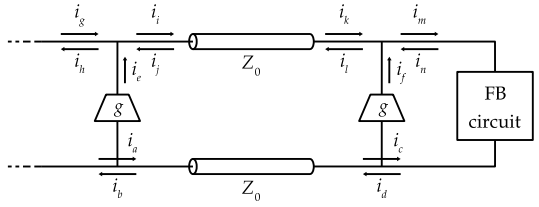


Figure 2.31: Currents in a two-section distributed amplifier with internal feedback.

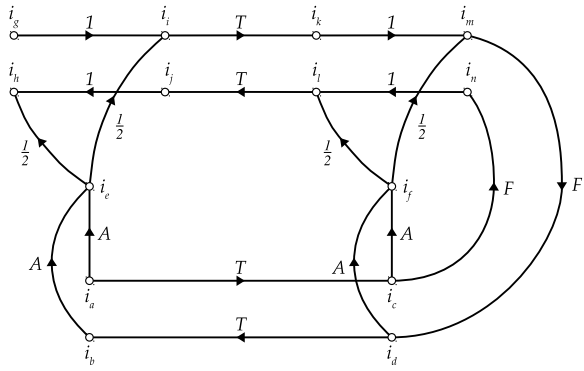


Figure 2.32: Signal flow graph of the two-section distributed amplifier with internal feedback.

as the *state variables* and are represented by nodes in the SFG. Note that forward and backward currents are being considered separately. It is assumed that the gate and drain transmission line sections all have the same characteristic impedance Z_0 and all present the same delay t for a current travelling through it. In the Laplace domain, this delay can be expressed as

$$T = e^{-st}. \tag{2.28}$$

The feedback path is represented by a transfer function F. It can be a simple transmission line section, presenting a delay, or a filter circuit with a more complex transfer function.

Figure 2.32 depicts the SFG of the circuit. As mentioned above, the currents in the amplifier are represented in the SFG by nodes. The directed branches represent the relationships between the currents. The time delay T and the feedback circuit transfer function F discussed above are indicated on the graph, as well as the current gain of each amplifier stage, given by

$$A = -Z_0 \cdot g e^{-sa}, \tag{2.29}$$

where g is the transconductance of a gain cell and a is its delay. The output current of each gain cell splits evenly between a right-bound part and a left-bound part; hence the factors $\frac{1}{2}$. The input of the amplifier corresponds to i_a, and the output corresponds to i_h. In a practical implementation the actual input may differ from i_a as there will likely be an extra transmission line section in between. This however merely results in a time delay and is therefore neglected in this analysis.

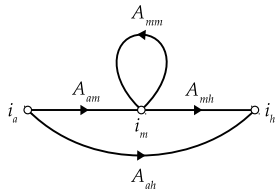


Figure 2.33: Reduced signal flow graph of the two-section distributed amplifier with internal feedback.

Using the techniques explained by Mason [Mas53b], the signal flow graph can be simplified to the one shown in Figure 2.33. The following expressions can be readily obtained for the transfer functions in the reduced SFG:

$$A_{mm} = F\left(A\frac{1}{2} + TA\frac{1}{2}T\right) = \frac{1}{2}AF\left(1+T^2\right) \tag{2.30}$$

$$A_{am} = A\frac{1}{2}T + TA\frac{1}{2} = AT \tag{2.31}$$

$$A_{mh} = F\left(A\frac{1}{2}T + TA\frac{1}{2}\right) = AFT \tag{2.32}$$

$$A_{ah} = A\frac{1}{2} + TA\frac{1}{2}T + TFT = \frac{1}{2}A + \frac{1}{2}AT^2 + FT^2 \tag{2.33}$$

These expressions can be generalized for a distributed amplifier of N stages:

$$A_{mm} = \frac{1}{2}AF\sum_{k=0}^{N-1} T^{2k} \tag{2.34}$$

$$A_{am} = \frac{N}{2}AT \tag{2.35}$$

$$A_{mh} = \frac{N}{2}AFT \tag{2.36}$$

$$A_{ah} = \frac{1}{2}A\sum_{k=0}^{N-1} T^{2k} + FT^{2(N-1)} \tag{2.37}$$

A_{am} is simply the (current gain) transfer function of a classic distributed amplifier without internal feedback, corresponding with (2.1). A_{mm} is the sum of all loop gains. The input-output transfer function of the graph shown in Figure 2.33 is given by

$$\frac{i_h}{i_a} = A_{ah} + \frac{A_{am}A_{mh}}{1-A_{mm}}. \tag{2.38}$$

Referring again to Figure 2.31, the current i_m is fed back to the input line of the amplifier and is amplified a second time. However, in addition to the desired forward-amplified current i_h, also a reverse-amplified current is generated, flowing to the right. This current again passes through the feedback network and is well on its way to be amplified over and over again. This raises serious questions about stability. As the authors claim the

feedback increases the gain of the amplifier, it *must be positive* and therefore inherently unstable. The paper makes only a reference to stability in passing, mentioning that the input and output distributed amplifiers provide stability. These are conventional distributed amplifiers that have been placed before and after the amplifier with internal feedback. It is not clear how these can improve the stability of the amplifier with internal feedback.

The publication does however show a filter in the feedback path which might be crucial to maintain stability. From the discussion above, it should be clear that instability is due to the undesired reverse-amplified signals. As discussed in Section 2.3.1, the reverse gain shows large peaks at DC and above the cut-off frequency of the artificial transmission lines, and is small mid-band. This suggests it might be possible to use a high-pass filter in the feedback network so that the frequencies where the reverse gain is large are suppressed. While Arbabian and Niknejad do not discuss the nature of the filter, the gain plot in the paper shows a band-pass shape, indicating that it could indeed be a high-pass filter.

2.5 Conclusion

The concept of distributed amplification enables the realization of amplifiers featuring very large gain-bandwidth products, with amplifiers in literature showing bandwidths near 100 GHz. This is achieved by operating transistors in parallel and separating their parasitic capacitances by absorbing them in artificial transmission lines, LC ladders or capacitively-loaded transmission lines. In monolithic distributed amplifiers, these transmission lines are approximated by LC ladders or periodically-loaded planar transmission lines. These can only approximate transmission lines up to a certain frequency, which determines the bandwidth of the amplifier. The properties of the LC ladder and the periodically-loaded transmission line are very similar. For example, they both show peaking near the cut-off frequency, which helps to compensate for skin-effect losses.

Losses in the artificial transmission lines and parasitics in the transistors negatively affect the operation of the distributed amplifier. Series losses in the inductors or transmission lines and shunt losses associated with the transistors limit the amount of sections and the maximum attainable gain. The feedback capacitance C_{gd} of field-effect transistors severely affects the bandwidth and stability of the distributed amplifier. More complex gain cells, such as the cascode, can be used to mitigate the Miller effect and reduce the effect of the feedback capacitance.

Noise in the distributed amplifier is mainly due to the gain cells and the input-line termination resistor. The contribution of the latter to the output noise is suppressed mid-band by the reverse gain of the distributed amplifier. At DC, the noise of this termination resistor limits the noise figure of the amplifier to a minimum of 3 dB. Linearity of the distributed amplifier benefits from the transistors being operated in parallel and therefore offers an advantage compared to cascade amplifiers.

The distributed amplifier has also spawned a number of similar topologies. The cascaded single-stage distributed amplifier is basically a cascade of single-stage distributed amplifiers, capable of obtaining a higher gain thanks to the multiplicative gain. How-

ever, the left part of each interstage transmission lines is omitted; the stages no longer strictly operate as distributed amplifiers and optimization is required to obtain a flat frequency response. The matrix amplifier stacks two or more distributed amplifiers to also make use of the reverse currents, increasing the gain. However, this results in a strongly frequency-dependent gain response, also requiring optimization to obtain a flat frequency response. Tapering of the distributed amplifier's output transmission line does not disturb the flat gain response, but eliminates the left-hand termination resistor, doubling the output current. For the same bandwidth, the load impedance needs to be reduced however, with a factor equal to the number of stages. Finally, the distributed amplifier with internal feedback is without doubt the most intriguing topology. The input signal passes through the amplifier twice, increasing the gain significantly.

Chapter 3

Low-Power Distributed Amplifier Design Techniques

Distributed amplifiers are generally considered to be rather power-hungry. Part of this negative image is due to the fact that the bulk of distributed amplifiers presented in the literature are designed to obtain the maximum attainable gain-bandwidth product. This automatically leads to maximum transconductance biasing and a high power consumption. Different design criteria can help to keep the power consumption of a distributed amplifier to a minimum.

Nevertheless, the fact remains that the additive nature of the distributed amplifier's gain provides less gain for a given number of stages compared to the multiplicative gain in cascade amplifiers. More importantly, half of the output signal power is lost in the left-hand termination resistor; this is the most important factor limiting the power efficiency of a distributed amplifier.

Despite the limitations of the topology, Zhang and Kinget presented a low-power distributed low-noise amplifier (DLNA) that holds up quite well against broadband LNAs based on other amplifier topologies [Zha06]. This is however one of only a few publications on low-power distributed amplifier design.

This chapter focuses on further reducing the power consumption of the distributed amplifier. As the tapered distributed amplifier discussed in Section 2.4.3 allows eliminating the reverse waves and thus doubling the power efficiency, we take a closer look at this topology. A new tapering scheme is presented that allows increasing the load impedance of the tapered distributed amplifier. Also, a new amplifier topology is proposed, the tapered matrix amplifier, that combines the advantages of the tapered distributed amplifier and the matrix amplifier. Finally, a number of low-power techniques are discussed that can help to further reduce the power consumption of the tapered matrix amplifier.

3.1 Tapered Distributed Amplifier

Tapering the output transmission line of a distributed amplifier allows eliminating the reverse waves that are otherwise lost in the termination resistor. However, when using the tapering scheme discussed by Ginzton [Gin48], the load impedance needs to be lowered compared to that of a classic distributed amplifier with the same bandwidth, limiting the amplifier's gain. For a classic N-section distributed amplifier, the power

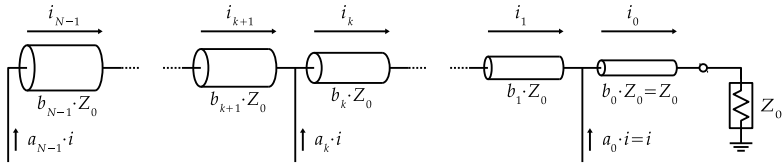


Figure 3.1: Tapered output transmission line of an N-section distributed amplifier. The $a_k i$ represent the currents injected into the transmission line by the distributed amplifier's gain cells.

gain is

$$G_p = \frac{N^2 g_m^2 Z_{0g} Z_{0d}}{4}. \tag{3.1}$$

where Z_{0g} and Z_{0d} are the characteristic impedances of the input and output transmission lines respectively. The power gain of the tapered distributed amplifier, which operates into a load that is N times lower (see Section 2.4.3), is given by

$$G_{p,\text{taper}} = N^2 g_m^2 Z_{0g} \frac{Z_{0d}}{N} = N g_m^2 Z_{0g} Z_{0d}. \tag{3.2}$$

As long as the number of sections N is smaller than 4, the tapered distributed amplifier's power gain is higher than that of the classic distributed amplifier. However, the load impedance must also be N times lower, which can prove troublesome when matching to another circuit. As broadband matching networks are often not an option due to their bulkiness and associated high loss, this is a major impediment to the tapered distributed amplifier's applicability. Even lossless matching networks are unable to provide a perfect match across a given bandwidth, and the quality of the match is inversely proportional to the bandwidth, as demonstrated by the Bode-Fano criterion [Poz05].

The tapered distributed amplifier discussed by Ginzton uses identical gain cells. In the following section, the general case for arbitrary gain cells is analyzed. Finally, the outcome of this analysis is used to propose an alternative tapering scheme that allows operating into a larger load impedance.

3.1.1 Generalized Theory

A primary requirement for the correct operation of the tapered distributed amplifier is that the respective delays between the inputs and outputs of the gain cells are equal (see Section 2.1). In the following derivation, we assume that this requirement is met, and concentrate on the correct tapering of the output transmission line sections. For this reason, and to not needlessly complicate the derivation, the phase information of the currents indicated in the figures has been omitted.

Figure 3.1 depicts a lossless tapered output transmission line of a distributed amplifier. The currents $a_0 i \ldots a_{N-1} i$ injected by the gain cells are expressed relative to a reference current i. Similarly, the characteristic impedances $b_0 Z_0 \ldots b_{N-1} Z_0$ are expressed relative to an impedance Z_0. Note that a_0 and b_0 have been chosen equal to 1. Figure 3.2

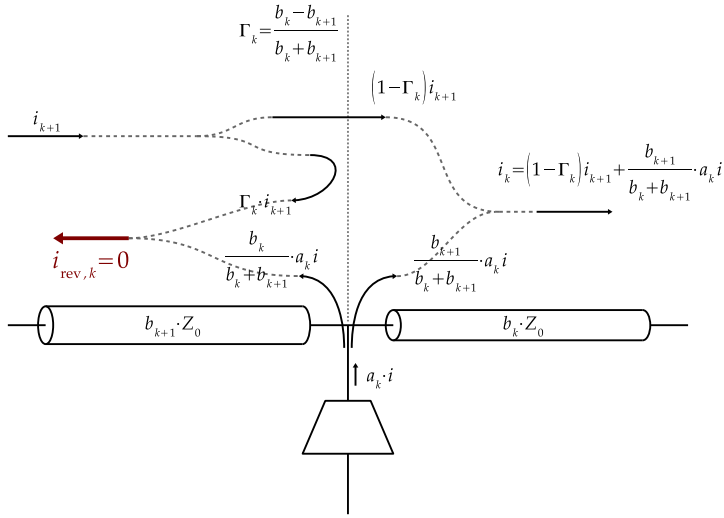


Figure 3.2: Representation of the reflected and transmitted currents at the interface between two sections of an output transmission line of a tapered distributed amplifier.

represents the current flow at the interface between transmission line sections k and $k+1$. The gain cell output current $a_k i$ splits up into a reverse (left-bound) part

$$\frac{b_k}{b_k + b_{k+1}} \cdot a_k i \tag{3.3}$$

and a forward (right-bound) part

$$\frac{b_{k+1}}{b_k + b_{k+1}} \cdot a_k i, \tag{3.4}$$

dictated by the characteristic impedances of the transmission line sections to the left and the right of the interface, $b_{k+1} Z_0$ and $b_k Z_0$ respectively.

When the current i_{k+1}, traveling down the left transmission line section, hits the interface, a part $\Gamma_k i_{k+1}$ is reflected, where Γ_k is the well-known voltage reflection coefficient from transmission line theory [Orf04] given by

$$\Gamma_k = \frac{b_k Z_0 - b_{k+1} Z_0}{b_k Z_0 + b_{k+1} Z_0} = \frac{b_k - b_{k+1}}{b_k + b_{k+1}}. \tag{3.5}$$

As tapering serves to eliminate any left-going currents, we require that the net reverse current vanishes:

$$i_{\text{rev},k} = \Gamma_k \cdot i_{k+1} + \frac{b_k}{b_k + b_{k+1}} \cdot a_k i = 0 \tag{3.6}$$

$$\Leftrightarrow (b_k - b_{k+1})\, i_{k+1} + b_k a_k \cdot i = 0 \tag{3.7}$$

Under this condition, the current i_{k+1} is equal to the sum of output currents of all of the gain cells to the left of the interface:

$$i_{k+1} = \sum_{m=k+1}^{N-1} a_m i = \left(S - \sum_{m=0}^{k} a_m \right) i \tag{3.8}$$

where

$$S = \sum_{m=0}^{N-1} a_m. \tag{3.9}$$

S multiplied by the reference current i is simply the total output current of the distributed amplifier (i_0 in Figure 3.1).

A general solution to (3.7) is given by

$$b_k = \frac{S}{\sum_{m=k}^{N-1} a_m} = \frac{S}{S - \sum_{m=0}^{k-1} a_m}. \tag{3.10}$$

This expression relates the currents injected by the gain cells to the characteristic impedances of the tapered transmission line sections required to eliminate all reverse currents. For the conventional tapering scheme where all transistors are equally sized ($a_k = 1$ and thus $S = N$), (3.10) reduces to

$$b_k = \frac{N}{N-k}. \tag{3.11}$$

Setting $k' = N - k$, we can see that the characteristic impedance of the transmission line sections indeed needs to decrease according to $1/k'$ from left to right. This is in agreement with the values obtained by Ginzton et al. [Gin48] and discussed in Section 2.4.3.

3.1.2 New Tapering Scheme

In distributed amplifiers, the characteristic impedance of the transmission line sections is closely linked to the input and output capacitance of the gain cells, as detailed in Section 2.1.1. In the conventional distributed amplifier, the transmission line sections all have the same characteristic impedance. The gain cell size and inductor values of an LC-ladder based implementation are easily determined using (2.6) and (2.3). In the tapered distributed amplifier, however, the characteristic impedance of the output transmission line sections needs to decrease toward the load, according to (3.10). In the conventionally tapered distributed amplifier, with identical gain cells, the characteristic impedance of the sections needs to decrease from left to right with $1/k'$, as discussed above.

It is important that the cut-off frequency (and delay) of the sections does not change when scaling the characteristic impedance of the lines. To this end, it is useful to write the LC ladder equations (2.3) and (2.6) in terms of the characteristic impedance:

$$L = Z_0^2 C \tag{3.12}$$

$$f_c = \frac{1}{\pi Z_0 C} \tag{3.13}$$

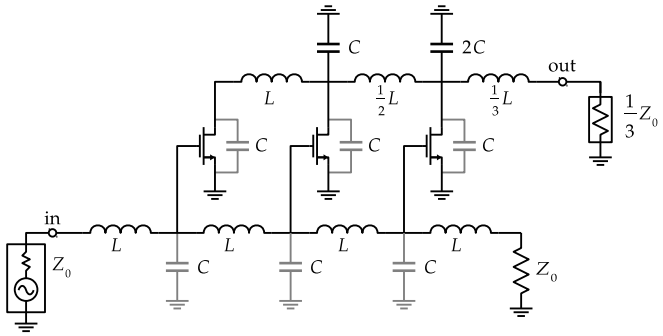


Figure 3.3: LC ladder implementation of a three-section tapered distributed amplifier using FET gain cells. Capacitors in gray represent the input and output capacitance of the FETs.

From (3.13), we can see that the capacitance in an LC ladder should decrease with increasing characteristic impedance in order not to lower the bandwidth of the amplifier. If L_0 and C_0 make up an LC ladder section with characteristic impedance Z_0, an LC ladder with the same cut-off frequency, and a characteristic impedance of $b_k Z_0$ requires inductors and capacitors with values

$$L_k = b_k L_0, \text{and} \tag{3.14}$$

$$C_k = \frac{C_0}{b_k}. \tag{3.15}$$

The smallest capacitance, corresponding to the largest characteristic impedance, in a conventionally tapered distributed amplifier output LC ladder is

$$C_N = \frac{C_0}{N}. \tag{3.16}$$

Since all gain cells are identical (all $a_k = 1$), C_N determines the sizes of all of the gain cells. To produce the other (larger) capacitances in the LC ladder, extra capacitance is placed in parallel with the gain cell's output capacitance [Che05]. We designate this as *passive* capacitance, since it does not bring extra gain to the amplifier as a transistor's capacitance does. Illustrating this, Figure 3.3 shows a three-section tapered distributed amplifier using FET gain cells that have input and output capacitance C. The two rightmost transistors have extra capacitance added at their outputs, C and $2C$ respectfully. Comparing the tapered distributed amplifier of Figure 3.3 to the classic non-tapered version using the same FET gain cells, we see that the load impedance is $\frac{1}{3}Z_0$, or $N = 3$ times lower than the load impedance of the classic distributed amplifier.

In order to create an extra degree of freedom in the design of the tapered distributed amplifier, we abandon the requirement for identical gain cells. Where in the conventional tapering scheme extra capacitance needs to be added to the output of the gain cells, we try to devise a tapering scheme where the gain cells provide exactly the capacitance required in the output transmission line. In this case, C_k is fully determined by the transistor's

size and is therefore closely linked to its gain and output current $a_k i$. Assuming identical biasing voltages[1], a transistor's transconductance to output capacitance ratio

$$\frac{g_{m,k}}{C_k} = \frac{a_k g_{m,0}}{C_0/b_k} = a_k b_k \frac{g_{m,0}}{C_0} \tag{3.17}$$

is constant for different transistor sizes[2]. As a_0 and b_0 have been chosen equal to 1, this implies that all $a_k b_k$ products should equal 1, imposing an extra constraint on the relative sizes of a_k and b_k, in addition to the requirement described by (3.10).

In the classic tapering scheme, the transistors are identical ($a_k = 1$ and $S = N$) and thus, from (3.11), $a_k b_k = b_k > 1$, indicating that extra capacitance needs to be added to the output transmission line indeed. To obtain $a_k b_k = 1$ and thus avoiding the need for additional capacitance at the output of the transistors, we set $a_k = 1/b_k$. The required a_k values can be readily derived from (3.10):

$$a_k = \frac{1}{b_k} = \frac{S - \sum_{m=0}^{k-1} a_m}{S} = \left(\frac{S-1}{S}\right)^k \tag{3.18}$$

Unfortunately, a problem appears for the left-most section. From (3.10), we find for $k = N-1$ that

$$b_{N-1} = \frac{S}{a_{N-1}} \tag{3.19}$$

and consequently

$$a_{N-1} b_{N-1} = S. \tag{3.20}$$

It is thus impossible to simultaneously satisfy both $a_{N-1} b_{N-1} = 1$ and the tapering condition given by (3.10). The value for a_{N-1} respecting (3.10) is given by

$$a'_{N-1} = S - \sum_{m=0}^{N-2} a_m. \tag{3.21}$$

Suppose we determine the size of the leftmost gain cell using (3.21), respecting the tapering requirement. From (2.3), we see that $a'_{N-1} b_{N-1} = S$ practically results in a lowered cut-off frequency $f_c/\sqrt{S}$ of the leftmost ladder section, upsetting the operation of the distributed amplifier. However, the deviation from ideal tapered operation can be minimized. Note that (3.18) is independent of the number of gain cells N. By increasing the number of cells, it is therefore possible to limit the required output current of the leftmost transistor ($a'_{N-1} g_{m,0}$). If the leftmost gain cell needs to contribute only a small part of the total output current, the impact on the amplifier's operation is limited. This is illustrated with an example in the next section.

We established that for the conventional tapering scheme, the load impedance is N times lower than for the non-tapered amplifier. In the proposed tapering scheme, the load is the same as in the non-tapered amplifier. For the same total output current $S \cdot i$, and thus the same power consumption, the new tapering scheme allows driving an S times larger

[1] The transistors' input and output terminals are respectively all at the same DC potential.

[2] This is closely related to the notion of a transistor's unity current gain frequency $f_T = \frac{g_m}{2\pi C_{\text{in}}}$ [San06].

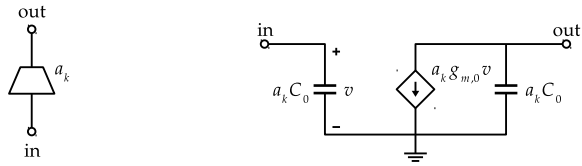


Figure 3.4: Gain cell: (a) symbol, and (b) circuit

Table 3.1: Values required for all a_k, b_k and a'_{N-1} for $S = 3$. These have been calculated using (3.18), (3.10) and (3.21), respectively.

k	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
a_k	**1.00**	**0.67**	**0.44**	**0.30**	**0.20**	0.13	0.09	0.06
b_k	1.00	1.50	2.25	3.38	5.06	7.59	11.39	17.09
N		**2**	**3**	**4**	**5**	**6**	**7**	**8**
a'_{N-1}		2.00	1.33	0.89	0.59	**0.40**	0.26	0.18

load than the conventional tapering scheme, increasing the power gain and efficiency by a factor S. However, due to the decreasing size of the gain cells, more sections are required to obtain the same output current.

3.1.2.1 An Example

To illustrate the application of the proposed tapering scheme, the gain of a tapered distributed amplifier with $S = 3$ is evaluated. The gain cells are modeled by transconductance (g_m) cells with equal input and output capacitances $C_{\text{in}} = C_{\text{out}} = C$. The rightmost gain cell is the reference cell ($a_0 = 1$) and has $g_m = 50$ mS and $C = 160$ fF. Later in this section, the gain cells in the amplifiers are represented by the symbol shown in Figure 3.4a. Figure 3.4b shows the corresponding circuit.

In order to obtain a 50 Ω characteristic impedance, the reference inductance L_0 should equal 400 pH. Applying (2.3), the cut-off frequency f_c is determined to be about 40 GHz. The theoretical power gain of the amplifier is

$$S^2 \cdot g_m^2 \cdot Z_0^2 = 17.5 \text{ dB}. \tag{3.22}$$

For comparison, the power gain of a conventionally tapered amplifier with $S = N = 3$ is S times lower, or 12.7 dB.

Table 3.1 shows the a_k, b_k and a'_{N-1} values for $S = 3$. A six-section ($N = 6$) implementation limits the required output current of the leftmost gain cell to only

$$\frac{a'_{N-1}}{S} = \frac{0.40}{3} = 13\ \% \tag{3.23}$$

of the total current, limiting the negative effect of the excess capacitance in the leftmost section. Figure 3.5 shows the six-section amplifier with the leftmost section sized

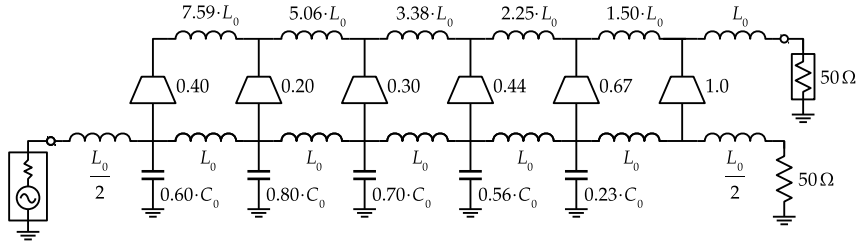


Figure 3.5: A six-section tapered distributed amplifier with $S = 3$. Not shown are series (proportional to the inductance value) and shunt losses. Note that extra capacitance needs to be added on the gate line.

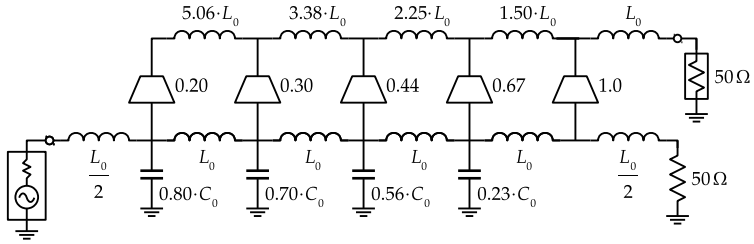


Figure 3.6: The distributed amplifier of Figure 3.5, but with the leftmost section removed.

according to a'_{N-1}. The small contribution of the leftmost cell allows omitting it without seriously affecting the operation of the amplifier. This configuration is shown in Figure 3.6. Figure 3.7 shows the gain of both configurations. The five-section amplifier indeed only shows a lower gain for frequencies roughly above $\frac{1}{3}f_c$, where the difference is small; the average gain drops by less than half a decibel on removing the leftmost section. Removing this section also removes the need for the largest inductance, $7.59 \cdot L_0$. Note that this is the inductance that is most difficult to realize in a monolithic implementation of the amplifier and takes up the largest die area.

Figure 3.7 also shows the gain of the conventionally tapered distributed amplifier with $N = 3$, that is, with the same total output current and thus the same power consumption. Due to the lower number of sections and their lower characteristic impedances, its decrease in gain due to losses is less than that of the amplifiers of Figures 3.5 and 3.6, slightly offsetting the gain advantage of the new tapering scheme. On the other hand, the conventional tapering scheme requires a load of $50/3\ \Omega$, typically requiring an impedance transformation network. And this is perhaps the most important advantage of the new tapering scheme, since broadband impedance transformation networks tend to be large and lossy [Rod09]. The added cost and attenuation due to an impedance transformation network can easily offset the advantages of the conventionally-tapered distributed amplifier.

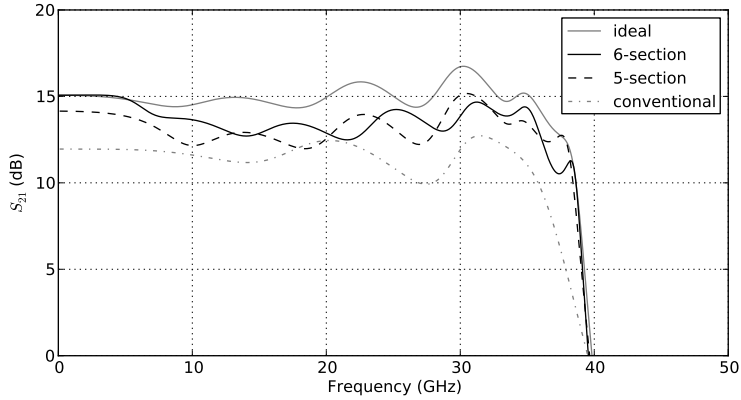


Figure 3.7: Comparison of the gain S_{21} of different variations on the six-section tapered distributed amplifier with $S = 3$; the ideal but physically non-realizable case, where the leftmost gain cell has a transconductance $0.40 \cdot g_m$ but only presents an output capacitance of $0.13 \cdot C_0$, the six-section amplifier of Figure (3.5), and the five-section amplifier of Figure 3.6. The gain of the conventionally tapered amplifier with $N = 3$ is also shown.

3.1.2.2 Practical Considerations

In contrast to the classic distributed amplifier, the operation of the tapered distributed amplifier depends on the relative magnitude and exact reflection of the output currents of the gain cells. In an idealized model built with lossless transmission lines, voltage-controlled current sources and no lumped capacitors, the reflections are exact and the amplifier's gain is perfectly flat, as expected from theory. For practical implementations, where at least the gain cell capacitors are lumped, this is no longer true. This also affects the classic distributed amplifier, but to a lesser extent since its operation only depends on the delays between gain cells being equal and not on the exact interaction of the gain cell output currents.

In the classic distributed amplifier, the output transmission line is uniform and can be fairly well approximated with an LC ladder or periodically-loaded planar transmission lines. In the tapered distributed amplifier, each line section has a different characteristic impedance and is typically approximated using only a single LC ladder section. Furthermore the sections are asymmetric, as the capacitor is located at the same point where the current is injected. These circumstances add to the crudeness of the transmission line approximation and this translates to a deviation from the flat frequency response. Additionally, losses affect the relative magnitudes of the output currents of the gain cells, also causing the amplifier operation to deviate from the ideal case. On a positive note however, losses help flatten the frequency response, demonstrated by Figure 3.7, showing a gain variation of only about 3 dB. Do note though that the circuit does not yet include the frequency-dependent (skin-effect) losses or transistor non-idealities (C_{gd}) one runs into in reality. In a practical design, the gain variation can be reduced by subjecting the circuit to optimization techniques. The latter is extensively discussed in

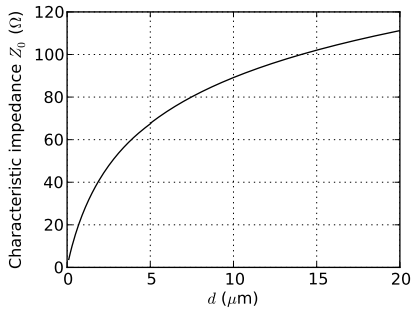


Figure 3.8: Approximate characteristic impedance [Poz05] of a microstrip line as a function of the spacing d between a 5 µm-wide signal conductor and ground plane for a typical CMOS process ($\varepsilon_r = 3.5$).

Chapter 4.

The main difficulty in the implementation of a tapered distributed amplifier is the realization of the high-characteristic-impedance transmission lines. In an LC ladder implementation, high-characteristic impedance sections require large inductors. The self-resonant frequency of planar inductors decreases with increasing inductance, ultimately limiting the bandwidth of the amplifier. Also, losses increase with increasing inductance, limiting the gain of the amplifier.

Similarly, it is difficult to create planar transmission lines with a high characteristic impedance in standard silicon processes. To illustrate this, Figure 3.8 shows the characteristic impedance of a microstrip line as a function of the spacing d between the signal conductor and the ground plane. While the characteristic impedance is inversely proportional to the width of the conductor, the width cannot be reduced indefinitely as losses need to be kept in check. Hence, the spacing d needs to be increased. In typical silicon processes, the height of the substrate stack allows for a spacing of only 2 to 6 µm, limiting the characteristic impedance. In addition, one should not forget that the capacitance of the gain cells decreases the effective characteristic impedance of the lines, so the initial characteristic impedance of the microstrip line will have to be even larger.

The situation is somewhat better for coplanar waveguides, where the gap is in the lateral direction and is not limited by the height of the substrate stack. The dimensions of the gap are still limited by practical considerations however, such as the need for the gain cells to connect both to the signal line and the ground conductors, only allowing a marginally higher characteristic impedance. The tapered distributed amplifier is therefore not immediately suitable for very wideband amplifiers which require planar transmission lines. Instead, it can offer a better efficiency for LC-ladder based distributed amplifiers.

3.1.3 Noise

In this section, we take a look at the noise properties of the tapered distributed amplifier. An obvious advantage of a tapered output transmission line is the elimination of the left-hand termination resistor and the associated thermal noise. However, the contribution due to that termination resistor is negligible compared to that of the other noise sources (Section 2.3.1). Therefore, it makes sense to take a close look at the other noise sources in the tapered distributed amplifier before getting too excited.

The calculation of the noise transfer functions of the other noise sources in the amplifier is complicated significantly by the presence of the tapered output line. The precise interaction of the currents on the output line is fulfilled only for the input signal and the noise source associated with the source impedance. The noise associated with the input line termination resistor and the gain cells is therefore subjected to reflections on the tapered output transmission line. This renders the noise analysis of the tapered distributed amplifier even more complicated than that of the classic distributed amplifier, and consequently, an expression modeling the noise performance is likely to be unwieldy.

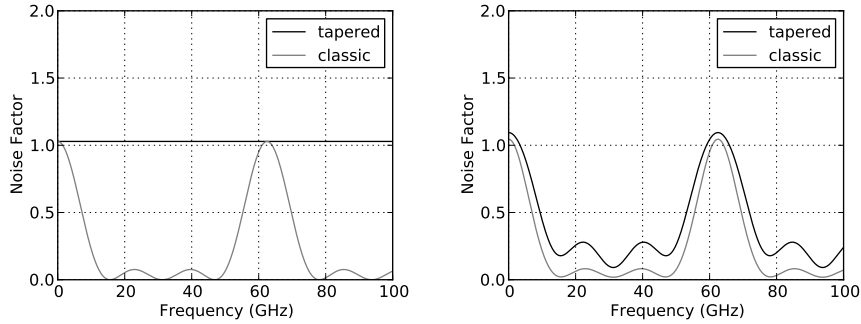
Let us take a closer look at the noise contribution of the input line termination resistor. As there is no left-hand termination resistor on the output transmission line, all of the noise power injected into the output line eventually ends up in the load. This is visible in Figure 3.9a, which shows the simulated contribution to the noise factor due to the input line termination resistor for both a classic (non-tapered) distributed amplifier and a tapered distributed amplifier. Both distributed amplifiers were simulated using ideal, lossless transmission lines and ideal voltage-controlled current source gain cells (no lumped capacitors). The noise factor of the classic distributed amplifier shows the distinct $\sin n\beta / \sin \beta$ shape[3]. The noise for the tapered amplifier is flat across the spectrum, as indeed all of the noise power at the output of the gain cells is destined to end up in the load. This seems to render the tapered distributed amplifier unsuitable for low-noise applications.

Introducing some losses into the output transmission line of the amplifiers in the form of 500 Ω shunt output resistance in each gain cell, the noise plot of Figure 3.9b paints a completely different picture. Indeed, for the lossless case, all of the noise power injected into the output line ends up in the load, but only after an infinite number of reflections. While they also contribute to the total output noise, these resistors allow for the reflected noise currents to get dissipated before they reach the load. Making the simplifying assumption that mainly the left-bound part of each gain cell's output current is dissipated by the shunt resistors, it is easy to see why the output noise due to the gate line termination resistor shows a similar shape to that of a classic distributed amplifier.

The level of the noise between the peaks in Figure 3.9b is closely linked to the sizes of the shunt resistors relative to the characteristic impedance. With the conventional tapering scheme, the shunt resistors need to be much smaller (higher losses) than with the new tapering scheme, since the characteristic impedance of the output transmission line sections are lower.

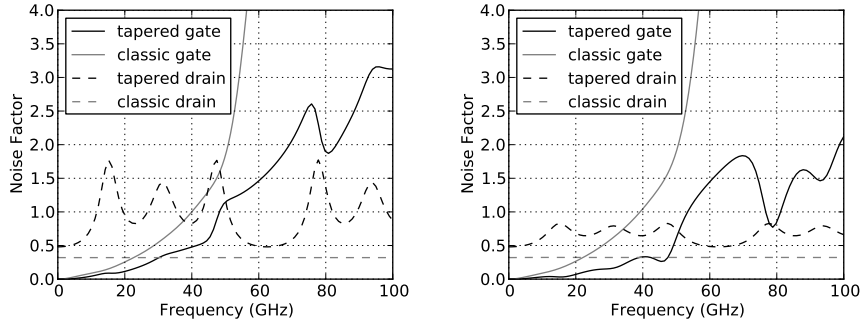
This positive effect of the losses on the noise performance of the tapered distributed

[3] This agrees with the derivation made by Aitchison, which is discussed in Section 2.3.1



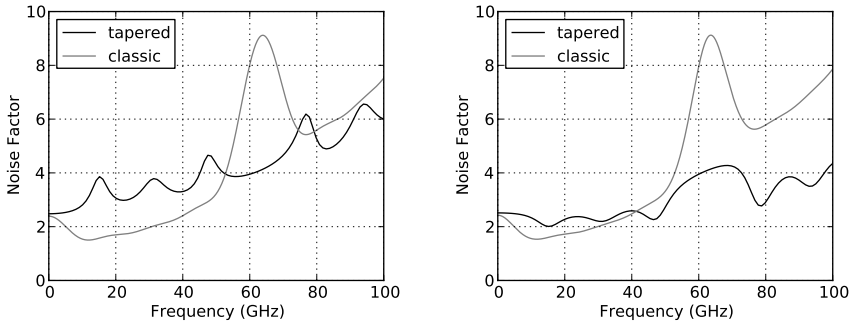
(a) (b)

Figure 3.9: Contribution to the noise factor by the gate termination resistor in a tapered distributed amplifier and the classic (non-tapered) distributed amplifier for (a) the lossless case, and (b) with a shunt resistance at the output of each gain cell. The tapered distributed amplifier uses the novel tapering scheme discussed in Section 3.1.2 with $S = 2$ and $N = 4$ to yield the same gain as the classic distributed amplifier of $N = 4$ stages.



(a) (b)

Figure 3.10: Contribution to the noise factor by the gate and drain noise current sources of the FET gain cells for (a) the lossless, and (b) the lossy tapered distributed amplifier .



(a) (b)

Figure 3.11: Tapered distributed amplifier noise factor for (a) the lossless case, and (b) the lossy case.

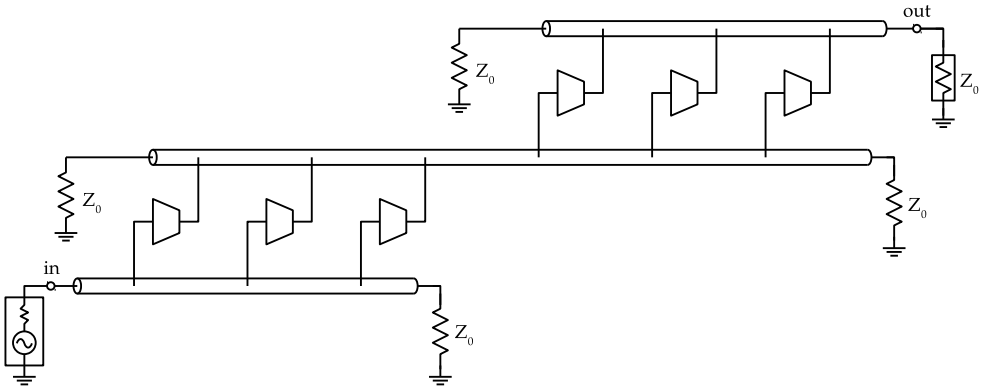


Figure 3.12: Two cascaded three-section distributed amplifiers. The long interstage transmission line causes significant attenuation.

amplifier also reduces the noise contribution due to the gain cells. Figure 3.10 shows the contribution to the noise factor by the gate and drain noise current sources of FET gain cells with and without losses on the output line. The total output noise is indeed reduced due to the presence of the losses. What's more, the noise due to the gate noise current sources is, even with a lossless drain line, lower than in the classic distributed amplifier. This is thanks to the fact that the gate-induced noise is proportional to the size of the FET. As the total size of the FETs in the tapered amplifier is half that of those in the classic amplifier, the noise generated by the gain cells is much less. This helps to keep the tapered amplifier's noise comparable to that of the classic distributed amplifier. Figure 3.11 shows the noise factor due to all noise sources for both the tapered and classic distributed amplifiers.

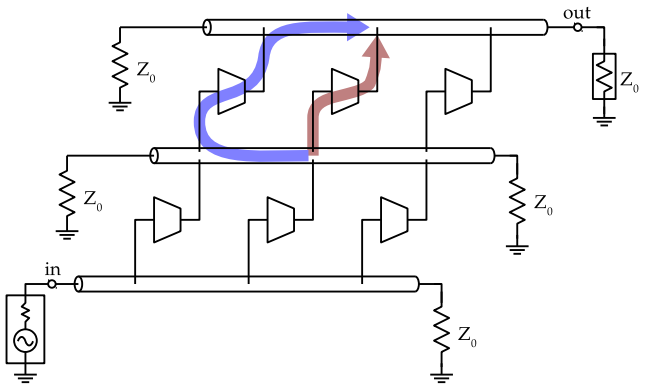


Figure 3.13: Signal flow in the matrix amplifier.

3.2 Tapered Matrix Amplifier

The additive nature of the gain of a distributed amplifier allows for very large bandwidths, but also limits the gain to power consumption ratio, or efficiency, of the amplifier. In order to improve the efficiency, several distributed amplifiers can be cascaded, as shown in Figure 3.12. A cascaded topology also allows some extra freedom in the design. For example, in a two-stage amplifier, the first stage can be optimized for noise [Fri44] while the second stage can be tuned for linearity. Unfortunately, the interstage transmission line formed by the output line of the first and the input line of the second amplifier is very long and considerably attenuates the signal.

The matrix amplifier discussed in Section 2.4.2 and shown in Figure 3.13 minimizes losses in the interstage transmission line by *stacking* the distributed amplifiers [Nic87]; the two stages now share a single short transmission line. In addition to minimizing signal attenuation, the shared line also occupies less area due to the reduction in the amount of transmission line sections. Another advantage is that the gain of the matrix amplifier is higher than that of the cascaded DA, as also the backward-traveling signals on the interstage transmission line are amplified by the second stage gain cells. But the matrix amplifier also introduces a new problem. Due to the existence of backward waves on the interstage transmission line, the gain of the matrix amplifier is frequency dependent. While the non-flat frequency response can be compensated by means of circuit optimization techniques, it would be preferable to eliminate the reverse waves, restoring the flat gain response and allowing better insight into the operation of the amplifier. It so happens that elimination of the reverse currents has been covered extensively in Section 3.1. The tapered matrix amplifier [Mac12], shown in Figure 3.14, does not suffer from the frequency-dependent gain that troubles the matrix amplifier.

As the output current of, for example, gain cells 12 and 13 does not pass the input of gain cell 21, one might expect that the gain of the tapered matrix amplifier is lower than that of an amplifier in which the two three-section stages are cascaded in series (not stacked). On closer inspection, we find that this is not true. Referring again to Figure 3.1, the voltage v_k on the kth section of a tapered distributed amplifier output transmission line

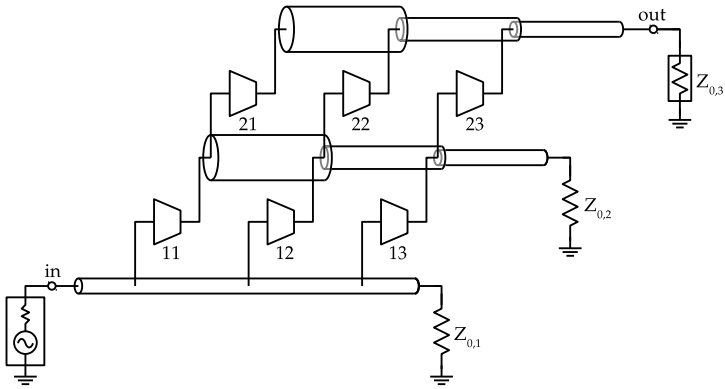


Figure 3.14: The tapered matrix distributed amplifier does not exhibit multiple amplification paths with unequal delays.

is given by the product of the current flowing through it and its characteristic impedance. Using (3.8) and (3.10), we find that

$$v_k = \left(\sum_{m=k}^{N-1} a_m i \right) \cdot b_k Z_0 \tag{3.24}$$

$$= S \cdot i \cdot Z_0 \tag{3.25}$$

This expression is independent of k and thus equal for all sections. Indeed, the continuity of fields[4] and the absence of left-going waves implies that the voltage is identical in all sections of the tapered transmission line[Orf04]. Therefore, the voltage at any point on the line is equal to the output voltage, implying that the input voltages to the second-stage gain cells are the same whether connecting the two DAs in series or in the tapered matrix structure. The gain of the tapered matrix amplifier is therefore the same as that of the cascade of the individual stages. A nice bonus, indeed! The voltage gain of the amplifier in Figure 3.14 is then given by the product of the gains of the individual tapered amplifiers:

$$\sum_{k=1}^{3} g_{m,1k} Z_{0,2} \cdot \sum_{k=1}^{3} g_{m,2k} Z_{0,3}. \tag{3.26}$$

But surely, it can't all be good news. The output capacitance of the first-stage gain cells and the input capacitance of the second-stage cells add, limiting the characteristic impedance of the interstage transmission line. But the situation is not as bad as it might seem. The examples in this dissertation have so far assumed that the output capacitance of the gain cells equals the input impedance. However, in MOSFETs for example, the output capacitance is only about half of the input capacitance, so the size of the lumped capacitances on the interstage line is not double that of the capacitance on the input line. In addition, as the size of the transistors decreases toward the left, the second-stage

[4]The sum of the voltages of the incident and reflected waves at a transmission line intersection is equal to that of the transmitted wave [Sil84].

amplifier can be shifted one position to the right, also reducing the size of the lumped capacitance at each node. This comes at the cost of an extra interstage transmission section, increasing losses and required die area, however.

3.3 Low-power Techniques

In addition to the use of the new tapered matrix topology, some additional techniques can be applied to the design of a distributed amplifier to minimize its power consumption. These are discussed in the following sections.

3.3.1 High-Characteristic-Impedance Interstage Lines

The transmission lines in a distributed amplifier typically have a characteristic impedance of 50 Ω to match the source and load impedances. The interstage transmission line in a cascaded distributed amplifier is not subject to this requirement. Since gain cells in a distributed amplifier are of the transconductance type (BJTs or MOSFETs), increasing their load impedance increases their output voltage. Hence, increasing the characteristic impedance of the interstage transmission line increases the input voltage to the gain cells of the second stage and thus the overall gain of the amplifier [Ban00, Tsa05, Par06a]. This is reflected in the voltage gain expression (2.1) of the distributed amplifier.

One can also look at this in terms of power matching. As their input and output capacitances are absorbed into the artificial transmission lines, the gain cells have real input and output impedances. For FET gain cells, these are typically very large. Increasing the characteristic impedance of the artificial transmission lines brings them closer to power matching with the gain cells, resulting in more power transferred and thus a higher gain.

We should not forget that the characteristic impedance of a transmission line section is closely linked to the size of the active devices (see Section 3.1.2). When the characteristic impedance is doubled, the device sizes need to be halved, also halving their transconductance. Hence, there is no net increase of the output voltage. However, the bias currents and thus also the power consumption are reduced by 50 %, effectively doubling the efficiency of the gain cells. Finally, an increased characteristic impedance requires larger inductors or planar transmission lines with a larger characteristic impedance. As with the tapered distributed amplifier, the practical limitations of monolithic integration limit the maximum characteristic impedance.

3.3.2 High-Characteristic-Impedance Input Line

The characteristic impedance of the input transmission line can also be increased to the same end. However, the input transmission line is subject to an extra constraint; its characteristic impedance should match the source impedance to avoid reflections. Ideally, if the amplifier's input is directly connected to an antenna, the latter could be designed to have an increased antenna impedance that is equal to the increased

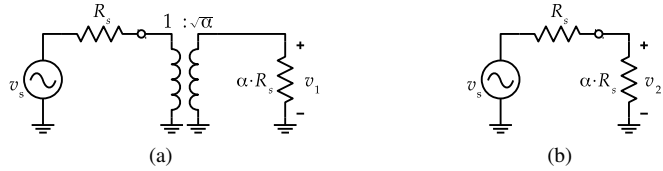


Figure 3.15: (a) Use of a matching network versus (b) a direct connection.

input impedance. Alternatively, an impedance transformation network[5] can be inserted between the source (typically 50 Ω) and the LC ladder input. On the other hand, broadband impedance transformation networks (e.g. transformers, multi-section or tapered transmission lines) are bulky and attenuate the signal. An alternative option is to simply omit the impedance transformation network. This does not have any detrimental effects on the antenna operation other than part of the inbound power being reflected. Also, the voltage at the input of the amplifier is lower compared to when an impedance transformation network is used. However, it can be shown that this decrease in input voltage is very small in practice.

The voltage across a load αR_s connected to a source with internal resistance R_s via an ideal matching network (Figure 3.15a) is

$$v_1 = \frac{\sqrt{\alpha}}{2} v_s, \tag{3.27}$$

where v_s is the open-circuit voltage of the source. The voltage across the same load αR_s when connected directly to that source (Figure 3.15b) is

$$v_2 = \frac{\alpha}{1+\alpha} v_s. \tag{3.28}$$

The ratio of these is given by

$$\frac{v_2}{v_1} = \frac{2\sqrt{\alpha}}{1+\alpha}. \tag{3.29}$$

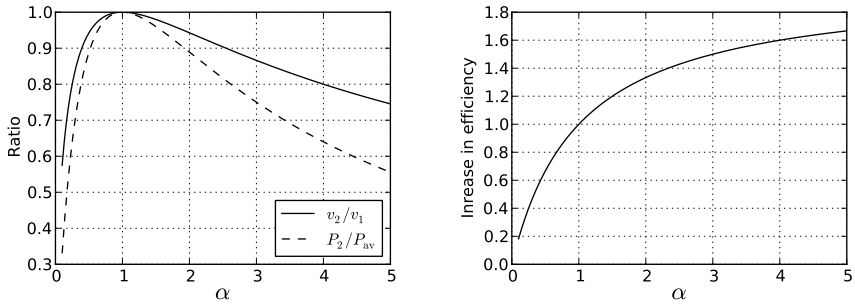
Table 3.2 shows the value of this ratio for different values of α. For values of α close to 1, (3.29) is close to 1. For example, the voltage across a 100 Ω load directly connected to a 50 Ω source ($\alpha = 2$) is only 6 % lower compared to when an ideal impedance matching network is inserted; not dramatic at all. Also the power dissipated in the load does not drop steeply with increasing values of α. When the load is matched ($\alpha = 1$), the power dissipated in the load is the available power

$$P_{\text{av}} = \frac{\hat{v}_s^2}{8R_s}, \tag{3.30}$$

[5] Broadband impedance transformation networks can be implemented using transformers, but these are not always able to provide enough bandwidth. An alternative option is a tapered transmission line [Col01]. Both require a large die area and introduce additional losses.

Table 3.2: Voltage across a load impedance αR_s connected to a power source with internal impedance R_s with (v_1) and without (v_2) an ideal matching network. Also shown are their ratio v_2/v_1 and the ratio of the power dissipated in the load without matching network P_2 to the available power P_{av}.

α	0.5	1	2	3	4	5
v_1/v_s	0.35	0.50	0.71	0.87	1.00	1.12
v_2/v_s	0.33	0.50	0.67	0.75	0.80	0.83
v_2/v_1	0.94	1.00	0.94	0.87	0.80	0.7
P_2/P_{av}	0.89	1.00	0.89	0.75	0.64	0.56



(a) (b)

Figure 3.16: (a) Voltage and power ratio's of the unmatched to the lossless matched case. (b) The gain-to-power-consumption ratio as a function of α

assuming a sinusoidal source voltage with amplitude $\hat{v}_s$. Using 3.28, the power dissipated in a load αR_s is

$$P_2 = \frac{\hat{v}_2^2}{2\alpha R_s} = \frac{4\alpha}{(1+\alpha)^2} P_{\text{av}}. \tag{3.31}$$

The ratio P_2/P_{av} as a function of α is also listed in table 3.2. Both the voltage and power ratios are plotted in Figure 3.16a. For small α larger than 1 ($\alpha \leq 3$), there is little to be gained by including an impedance transformation network, since it does not improve the amplifier's gain significantly. In fact, due the losses present in a broadband impedance transformation network, the net gain could even be lower. Only for larger loads, the use of a matching network becomes more favorable. Finally, note that the matching network can only be omitted if there is no component (e.g. duplexer, filter) between the antenna and the amplifier that requires proper termination [Hua99].

Increasing the input transmission line's characteristic impedance to α times the source impedance increases the distributed amplifier's input voltage according to

$$\frac{v_2}{v_{2,\alpha=1}} = \frac{2\alpha}{1+\alpha}, \tag{3.32}$$

compared to when the input transmission line's characteristic impedance equals the

source impedance. For $\alpha = 2$, (3.32) evaluates to $4/3$, an increase of 33 %. However, as discussed in Section 3.3.1, the device sizes need to halve when doubling the input transmission line's characteristic impedance. The gain and power consumption of the devices are halved but the input voltage is not doubled as is the case for an interstage transmission line, reducing the net gain. In general, the transconductance of the amplifier scales with the reciprocal of α, decreasing the net voltage gain according to

$$\frac{1}{\alpha} \cdot \frac{2\alpha}{1+\alpha} = \frac{2}{1+\alpha}. \tag{3.33}$$

However, the power consumption decreases at the same rate as the transconductance and thus the gain-to-power-consumption ratio, or efficiency, increases according to

$$\alpha \cdot \frac{2}{1+\alpha} = \frac{2\alpha}{1+\alpha}. \tag{3.34}$$

This relation is shown in Figure 3.16b. For $\alpha = 2$, the net gain decreases by one third and the gain-to-power-consumption ratio is increased by 33 %.

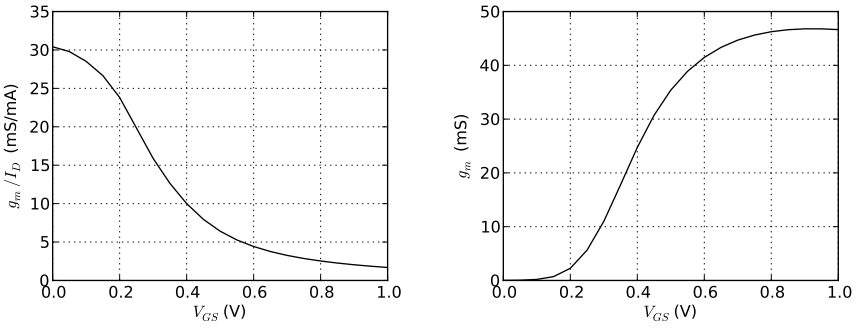
3.3.3 Gain Cell Selection

Most distributed amplifier designs employ cascode gain cells instead of single-transistor (common-source) gain cells to improve reverse isolation. In addition, they offer some advantages that were discussed in Section 2.2. But all these advantages come at the cost of an increased power consumption; the addition of the common-gate transistor roughly doubles the required supply voltage compared to a single transistor, and thus also consumes twice the power. The gain is not increased, as the transconductance is not altered by the addition of the common-gate transistor.

Only at very high frequencies, the feedback capacitance of a single-transistor gain cell will appear as a short-circuit and lead to instability. Therefore, for distributed amplifiers that need to operate over a very large bandwidth, single-transistors cannot provide sufficient reverse isolation and cascode gain cells need to be employed. However, depending on the application's gain and bandwidth requirements, common source gain cells might still provide sufficient reverse isolation, at roughly half the power consumption.

3.3.4 Biasing

A MOSFET's transconductance g_m to bias current I_D ratio drops with increasing gate-source voltage [San06], as shown in Figure 3.17a. Therefore, for low-power applications, it is advantageous to bias the MOSFETs toward weak inversion, as was done by Zhang and Kinget [Zha06]. However, the transconductance also decreases with decreasing gate-source voltages, shown in Figure 3.17b. So, when using a low gate-source voltage, wide MOSFETs are required to realize adequate gain. This in turn increases the parasitic capacitance which determines the bandwidth of the LC ladder and of the amplifier accordingly; the maximum sizes of the MOS transistors are ultimately determined by the bandwidth requirement.



(a) (b)

Figure 3.17: (a) Transconductance-to-bias-current ratio g_m/I_D and (b) transconductance g_m as a function of the gate-source voltage V_{GS} for a MOSFET with $W = 16 \times 2.5$ µm, $L = 80$ nm, $V_{DS} = 1.2V$

However, as the gain cells are placed in parallel in a distributed amplifier, it is possible to make better use of the increased transconductance-to-current ratio for lower overdrive voltages. Decreasing the overdrive voltage while increasing the number of sections to retain the total gain, the efficiency of the distributed amplifier can be improved significantly. For example, the 90-nm NMOS transistor from Figure 3.17 biased at $V_{GS} = 0.8$ V provides a transconductance g_m of 46 mS and a drain current I_D of 18 mA. Halving g_m to 23 mS by reducing V_{GS} to 0.39 V reduces I_D to a mere 2.2 mA. To obtain the same gain, two transistors are needed, resulting in a total current of 4.4 mA. The net reduction of the DC current is thus 13.6 mA, corresponding to a saving in power dissipation of 75 %. Of course, in practice the number of gain cells is not easily doubled, resulting in more modest reductions in power consumption.

The chosen bias point of the gain cells also affects the noise and linearity performance of the amplifier. This should be kept in mind during the design. For example, The noise excess factor γ drops when biasing the MOSFETs towards weak inversion [Ted94]. On the other hand, the transistors needs to be made wider to achieve adequate gain, increasing induced gate noise. Linearity of the distributed amplifier is discussed in detail in Chapter 4.

3.4 Conclusion

The tapered distributed amplifier eliminates all left-bound currents in the output transmission line; all of the gain cells' output current is dissipated in the load, effectively doubling the output current. However, the conventionally tapered distributed amplifier must operate into a lower load impedance than the classic distributed amplifier. This limits the power gain and typically requires the use of a broadband impedance transformation network, which brings considerable attenuation and extra cost due to losses and bulk, respectively.

The reduced load impedance is due to the fact that in the conventional tapering scheme, the gain cells are identical; this requires placing extra capacitance in parallel with the output capacitance of the gain cells in order to achieve tapering of the LC ladder. To eliminate the need for this extra capacitance and be able to operate into the same load as the classic distributed amplifier, a new tapering scheme was introduced. This tapering scheme was derived with the help of an expression governing the correct operation of a tapered distributed amplifier with arbitrarily sized gain cells, also derived in this chapter. The new tapering scheme allows operating into the same load impedance as the classic distributed amplifier. Thus, for the same power consumption, the new tapering scheme can double the power gain of the classic distributed amplifier. However, the new tapering scheme suffers from two conflicting requirements with respect to the left-most gain cell, but the associated negative effect can be minimized. This is illustrated with a simple design example.

A qualitative noise analysis of the lossless tapered distributed amplifier reveals that the noise originating from the input line termination resistor is not favorably shaped by the reverse gain as in the classic distributed amplifier, raising serious worries about the noise performance of the tapered distributed amplifier. However, losses present in the tapered output transmission line dissipate a lot of the amplified input termination noise power and the tapered distributed amplifier eventually does benefit from a similar shaping as in the classic distributed amplifier. The gate noise current source of a FET is proportional to the transistor size. The output noise due to these noise sources is therefore smaller in the tapered distributed amplifier, as, for the same gain, the total size of the transistors can be half that of those in the classic distributed amplifier. Additionally, the output noise due to the gain cells is also suppressed by losses in the transmission lines, an effect which is not significant in the classic distributed amplifier. In conclusion, the noise performance of the tapered distributed amplifier is similar to that of the classic counterpart.

In order to further improve the gain-to-power consumption ratio, two distributed amplifiers can be cascaded, taking advantage of multiplicative gain. To avoid losses, the two stages can be stacked as in the matrix amplifier. When stacking tapered distributed amplifiers, the gain is still frequency-independent, offering a large advantage compared to the matrix amplifier.

The tapered distributed and tapered matrix amplifiers can benefit from a number of generic low-power techniques. A first of these is increasing the characteristic impedance of the transmission lines. Due to the transconductive nature of the gain cells used in distributed amplifiers, simply increasing the load impedance to the gain cells increases the gain. Increasing the characteristic impedance of the artificial transmission lines requires scaling down the gain cells, however. Consequently, there is no net increase in gain. Still, scaling down the gain cells also decreases their DC current and power consumption. Finally, the type of gain cells and their biasing should be carefully considered in the design of a low-power distributed amplifier.

Chapter 4

Tapered Matrix Amplifier Implementation

In this chapter, we look at the design and implementation of a low-power tapered matrix amplifier (TMA) in a 90 nm CMOS process. The presented design serves as a proof-of-concept; it does not aim to fulfill the specifications required for any particular application. The amplifier's specifications have been chosen to allow comparison with other broadband amplifier topologies. First, the target bandwidth of the amplifier is 20 GHz, which is at the limit of what is attainable with non-distributed amplifier topologies. Second, the prototype should demonstrate a high gain, let's say 15 dB, to illustrate the strengths of the tapered matrix amplifier. In addition to these, the lowest possible power consumption is pursued.

The design of the amplifier is complicated by a number of non-idealities that interfere with the correct operation of the distributed amplifier, disturbing the flat gain response. Therefore, a pragmatic approach using circuit optimization is presented, to restore the flat gain response.

4.1 High-Level Design

First, a simple circuit model of the TMA is constructed. Problematic points in this circuit are identified, and by mutating the circuit topology, more room for optimization is created. The model of the mutated amplifier is used to determine the initial component values. Finally, carefully chosen constraints steer the optimizer to the final component values.

4.1.1 Topology Selection and Mutation

The prototype should ideally combine all of the low-power techniques discussed in Section 3.3. This implies a combination of an increased characteristic impedance and tapering of the interstage transmission line, requiring transmission line sections with a very high characteristic impedance. In order to limit the largest required characteristic impedance, the number of sections in each stage of the tapered matrix amplifier is limited to two. Figure 4.1 shows the resulting topology.

Like the interstage line, also the input line's characteristic impedance is doubled to benefit from the associated increase in efficiency. The output line's characteristic impedance is not increased from 50 Ω so as not to complicate the measurements and allow for fair comparison with other amplifiers. However, in RFIC design where one is not limited to 50 Ω impedances, it can make sense to opt for an increased characteristic

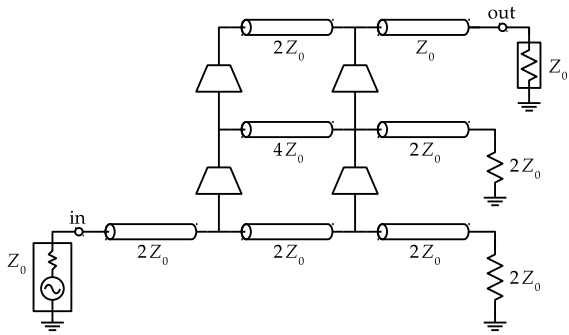


Figure 4.1: The tapered matrix amplifier topology selected for the prototype amplifier design. The source and load impedances are $Z_0 = 50\ \Omega$.

impedance. Finally, as the new tapering scheme discussed in Section 3.1.2 requires the contribution of the leftmost gain cell to be small, it cannot be used in a two-section amplifier. The lines are tapered assuming equally-sized gain cells.

4.1.2 First-Order Model

With a reference impedance of $Z_0 = 50\ \Omega$, the highest characteristic impedance of a transmission line section in Figure 4.1 equals 200 Ω, eliminating the possibility of an implementation using planar transmission lines (see Section 2.1.2). The circuit realization of the amplifier of Figure 4.1 employing common-source gain cells and lumped inductors is shown in Figure 4.2. The circuit reveals a potential problem with a practical implementation of the amplifier; the leftmost node of the interstage LC ladder allows for a capacitance of only $C/4$ while both the output of a first-stage transistor and the input of a second-stage transistor connect there. Adding an extra section to the interstage ladder, we obtain the revised amplifier topology of Figure 4.3, moving the first- and second-stage transistors to separate nodes, allowing them to be larger. Note that the extra section in the interstage LC ladder does not require tapering as no current is injected at the new interface. The extra section in the input LC ladder, required to have equal delays on the input and interstage lines, does require a capacitor to be inserted at node 12 due to the absence of a MOSFET gate, however. Figure 4.2 and 4.3 also show that the input LC ladder has been ended on both sides using inductor half-sections as this results in better characteristics (see Section 2.1.1).

The first-stage transistors in Figure 4.3 can have an input and output capacitance of respectively $C/2$ and $C/4$ respectively. MOSFETs suit this requirement nicely, in which the output capacitance C_{ds} is approximately half of the input capacitance C_{gs}. The second-stage transistors need to be half the size of the first-stage transistors, with an input capacitance of $C/4$. Their output capacitance is then on the order of $C/8$ and requires padding with additional capacitance to meet the tapering requirement. These padding capacitors have been indicated in Figure 4.3 in black.

The value for C, and thus the transistor sizes, is determined by the cut-off frequency of the LC ladders (2.3). As losses and the gate-drain capacitance reduce the bandwidth of

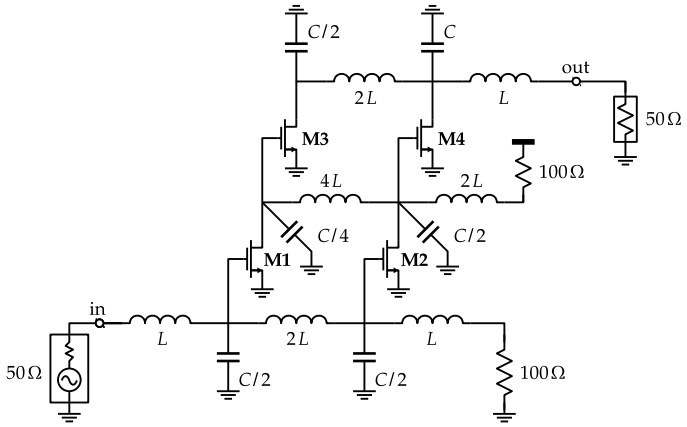


Figure 4.2: Circuit realization of the prototype tapered matrix amplifier employing MOSFET gain cells and lumped inductors. Indicated are the required relative sizes of the inductors and capacitors.

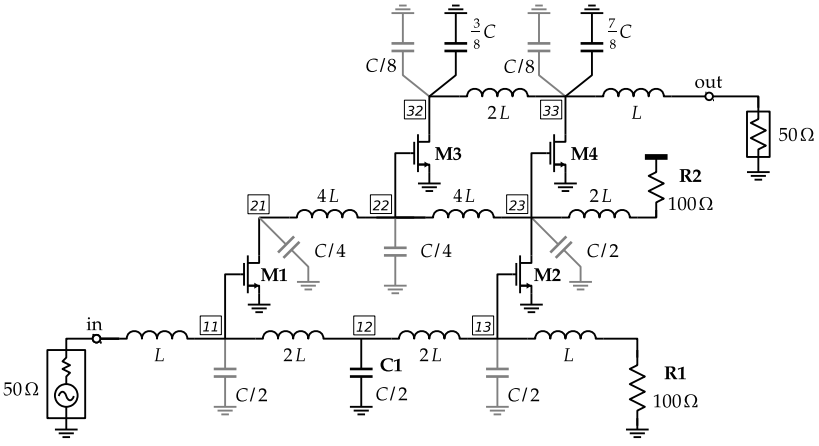


Figure 4.3: Revised circuit realization of the prototype tapered matrix amplifier. The extra section in the first-stage amplifier separates the output and input capacitance of M1 and M2 respectively. Capacitors in grey represent MOSFET input and output capacitance. Capacitors in black represent additional capacitance.

the distributed amplifier, a good initial choice for f_c is twice the target bandwidth:

$$C = \frac{1}{\pi Z_0 f_c} = \frac{1}{\pi \cdot 50\ \Omega \cdot 2 \cdot 20\ \text{GHz}} \approx 160\ \text{fF} \tag{4.1}$$

The smallest capacitance value $C/4$ is thus allowed to be 40 fF. The inductor values can be readily derived using (3.12):

$$L = Z_0^2 C = 400\ \text{pH}. \tag{4.2}$$

For now, we assume that both stages are biased identically. As the second-stage transistors are half the size of the first-stage transistors, a first-order expression for the voltage gain (between nodes *in* and *out*) of the amplifier in Figure 4.3 is given by:

$$A_v = \frac{4}{3}\left(2 \cdot g_m \cdot 100\ \Omega\right) \cdot \left(2 \cdot \frac{g_m}{2} \cdot 50\ \Omega\right), \tag{4.3}$$

in which the factor $\frac{4}{3}$ is due to the input mismatching discussed in Section 3.3.2. For a gain of 15 dB, the required g_m is 20 mS. The 90 nm CMOS transistors have a maximum unity-gain frequency f_T of about 135 GHz[1], corresponding to the ratio

$$\frac{g_m}{C_{\text{in}}} \approx 2\pi f_T = 0.85\ \frac{\text{mS}}{\text{fF}}. \tag{4.4}$$

The MOSFET in the amplifier, with $C_{\text{in}} = C/2 = 80$ fF, can thus have a maximum transconductance of approximately $g_m = 68$ mS. This provides generous headroom for compensating losses and allows to bias the transistors at a lower overdrive voltage to improve their efficiency. If this was not the case, a tapered matrix amplifier with more gain cells per stage or more stages is required.

4.1.3 Non-Idealities

There are a number of factors that cause the amplifier's operation to deviate from that of the theory discussed in the first chapters. First, as mentioned in Section 3.1.2.2, the approximation of the tapered transmission line with an LC ladder alters the operation of the tapered distributed amplifier. Second, losses, and in particular frequency-dependent (skin-effect) losses, also affect the gain flatness. Finally, in a distributed amplifier employing single-FET gain cells, the feedback capacitance C_{gd} has a large impact on the operation of the amplifier (see Section 2.2). The aggregate effect of these factors significantly complicate the design of the prototype amplifier. In order to cope with this complexity, a pragmatic approach embracing circuit optimization is taken in the design of the prototype, tuning the circuit components so as to obtain a flat gain response while also meeting the specifications.

Aiming for maximum efficiency however, we avoid adding extra "passive" capacitance at nodes 32 and 33, unless it is absolutely required. That is, the optimizer is configured to try and satisfy the optimization goals without adding extra capacitance. This may seem

[1] Unity current-gain frequency for a typical NMOS with $V_{GS} - V_T = 0.7 - 0.24$ V and $V_{DS} = 1.0$ V.

like an unorthodox approach to circuit design. However, it is important to note that the circuit already deviates significantly from its theoretical model due to the presence of the many non-idealities listed above. Furthermore, by removing some of the optimization constraints that ensure operation close to the theory, more degrees of freedom can be created in the optimization process. For example, it is not necessary for the individual gains of the two stacked distributed amplifiers to be flat across the frequency spectrum. It is only required that the net gain shows a flat frequency response. Not enforcing a flat frequency response of the individual stages gives the optimizer more maneuvering space to improve other specifications. In a way, this is similar to the approach taken by Niclas in the design of a matrix amplifier [Nic87]. However, in contrast to the matrix amplifier, the tapered matrix amplifier's gain is inherently flat and the deviation from it is only due to non-idealities.

4.2 Implementation Details

The following two sections cover the practical details of the optimization and layout of the amplifier.

4.2.1 Optimization

The circuit of Figure 4.3 serves as the starting point in the optimization process. The basic distributed amplifier operation is enforced by means of an optimization constraint specifying that the signal delays (phase) between the inputs and outputs of each pair of parallel gain cells should be equal. This requirement is enforced by directing the optimizer[2] to equalize the phase difference of the signals between the inputs and outputs of the parallel gain cells. That is, we require that:

$$\text{phase}\,(v_{21}, v_{23}) = \text{phase}\,(v_{11}, v_{13}) \quad \text{and} \tag{4.5}$$

$$\text{phase}\,(v_{32}, v_{33}) = \text{phase}\,(v_{22}, v_{23})\,, \tag{4.6}$$

where $\text{phase}\,(v_x, v_y)$ represents the phase difference between the voltages on nodes x and y. The node labels are indicated in Figure 4.3.

A second constraint ensures that the gain response of the amplifier is flat across the operating bandwidth. In theory, the equal-delay constraint should ensure a flat gain response, but the losses and other non-idealities discussed above invalidate this relation. Depending on the relative weight of the flat-gain and equal-delays constraints, the delays can diverge near the cut-off frequency of the amplifier. This is also the case in classic distributed amplifier designs [Tsa04, Chi07, Arb09], leading to increasing variations in the group delay at high frequencies[3].

Other constraints serve to enforce external requirements imposed by the amplifier's target specifications. These include, for the prototype amplifier, a flat gain of 16 dB[4] over 20 GHz. The optimization goal is to minimize the power consumption given these

[2] In the design of the prototype, the HSPICE built-in optimizer was used.

[3] In fact, it is impossible for lumped networks to provide a constant group delay [Lee04a].

[4] The extra decibel offers some margin to ensure that the measured IC meets the 15 dB gain requirement.

requirements. Other objectives can include noise figure and linearity, but these were not explicitly optimized in the prototype circuit. If they were, they would have to be weighted against other requirements such as gain and power consumption.

The following is a list of parameters that can be adjusted by the optimizer:

- spiral inductor geometry (number of turns, diameter, trace width and trace spacing)
- channel widths of the four MOS transistors
- the two termination resistor values R1 and R2
- DC (bias) voltages on the three LC ladders
- value of the capacitor on the input ladder C1

For the prototype design, the initial values for these parameters are based on the component values in Figure 4.3. Some of the design parameters are fixed to limit the optimization space; the number of inductor turns and the bias voltages on the input and output LC ladders. Also, the two $4L$ inductors in the interstage ladder share the same parameters, as do the two central ($2L$) and the two outer inductors (L) of the input LC ladder. In the case that the optimization fails to meet the design goals, some of these restrictions can be removed.

The availability of accurate models of all components is paramount in RF circuit design. Additionally, optimization requires parameterized models. The foundry design kit for the 90 nm process used in the prototype design included accurate models for all circuit components: MOSFETs (RF models), spiral inductors, resistors and capacitors, valid up to 20 GHz. The provided inductor models are macro-models based on on-wafer measurements and electromagnetic simulations and are therefore very accurate. Their parameters are: diameter, trace width, trace spacing and number of turns. In the event that no or inadequate inductor macro-models are provided by the foundry, they can be generated from sets of S-parameters obtained from EM simulations using commercially available tools, such as ADS Advanced Model Composer. Also for fully manual designs, it makes sense to generate these macro-models, as it helps the designer to explore the design space and speeds up iterations, which are inevitable in RF design.

4.2.2 Layout

The layout of the tapered matrix amplifier is less straight-forward than that of a classic distributed amplifier due to the extra row of devices and inductors of the second amplifier stage. The inductors could be arranged in a configuration similar to that of the circuit in Figure 4.3, but this makes it difficult to distribute the ground to the gain cells. The ground conductor would need to pass under the inductors or be routed around them. The former degrades the quality factor of the inductor. Using thin ground lines reduces the impact on the inductors, but degrades the quality of the ground connection. Similarly, routing the ground line around the inductors, increases the length of the ground conductor, increasing losses. For this reason, the inductors are organized in two rows, one above

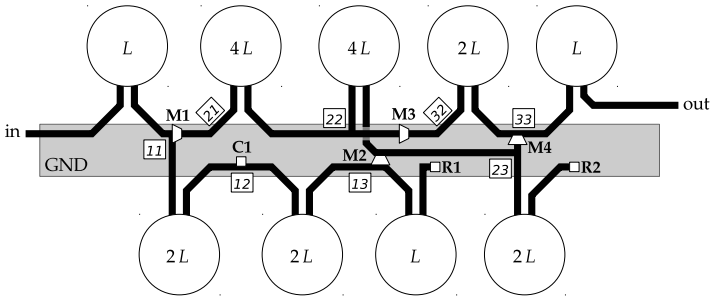


Figure 4.4: Schematic representation of the layout of the tapered matrix amplifier. The locations of the inductors, transistors, termination resistors and capacitor are indicated. The gray strip represents the ground plane which provides a good ground connection for the transistors and resistors.

and one below a wide ground strip that provides a good ground connection for the active devices. A disadvantage of this is that the inductors making up the *three* LC ladders need to be distributed across *two* rows, lengthening the interconnect between inductors mutually and to the active devices. To be able to accurately model this interconnect and still be able to optimize the inductor geometry, the inductors have been assigned fixed positions so that the interconnect network is independent of the optimization. The interconnect network was then simulated in ADS Momentum[5] [Tec06] to produce a 31-port S-parameter[6] model to be included during optimization, connecting the device models and macro-models of the inductors. The layout of the amplifier is schematically depicted in Figure 4.4. The locations of the spiral inductors to be optimized are indicated with circles. The gray strip in the background represents the ground plane that provides a good ground connection for the MOSFETs and resistors (for which cutouts have been provided). The ground plane is implemented in metal layer 1 and the inductors make use of the thick top metal. The devices connect to the inductors through tall via stacks, which have also been modeled using Momentum.

After optimization, the resulting values for the inductor geometry parameters were used to generate the layout of all the inductors together with the interconnect network in order to capture coupling effects. This structure was simulated in ADS Momentum, producing a 14-port S-parameter model. Replacing the inductor macro-models and interconnect model with the 14-port model, a final optimization step was performed to fine-tune the MOSFET and resistor sizes, to restore the flat frequency response and gain level of the amplifier. Figure 4.5 shows the final optimized values obtained for all components. The figure lists the total width of the NMOS transistors, each consisting of 16 fingers. For each inductor, the inductance at DC is given. The characteristic impedances and the termination resistances of the input and interstage LC ladders have been reduced from their initial values by the optimization process. Finally, the optimized value of capacitor C1 introduced in Figure 4.3 is 0 and can therefore be omitted.

[5] Appendix C discusses *Python-substratestack*, a software tool that aids in handling the substrate stack data required by EM field solvers.

[6] See Appendix A for notes on the use of S-parameters in a circuit simulator.

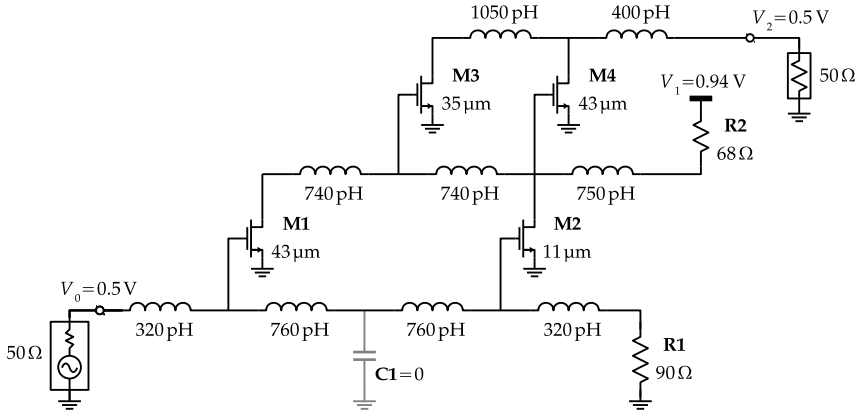


Figure 4.5: Final optimized values for the components in the amplifier; DC bias voltages, inductor values (at DC) and NMOS channel widths.

The optimized circuit consumes only 12.7 mW while meeting the gain and bandwidth requirements. More details about the circuit's performance are discussed in Section 4.3. Comparison with the state of the art show that this result is very competitive with designs based on the popular broadband low-power amplifier topologies.

On inspection of Figure 4.5 it is clear that the final component values differ significantly from the initial values in Figure 4.3. For example, M1 is almost four times as large as M2. Also, the inductors of the interstage ladder do not show significant tapering. It is however possible to see that the conditions for the transmission line tapering are still approximated. From the FET sizes in the first stage, $a_1 = W_{M2}/W_{M1} \approx 4$. According to (3.10), b_1 should be around 1.25. This clarifies the rather small inductance values of 740 pH (around $2L$) where much higher values ($4L$) are expected. Similarly, in the second stage, $a_1 \approx 0.8$ so that $b_1 = 2.25$, corresponding to a slightly larger than expected inductance value. It is also interesting to see that the optimization process reduced the value of the single passive capacitance $C/2$ introduced in Figure 4.3 to zero, supporting the idea that better overall performance can be achieved if all capacitance is provided by the gain cells. While the operation of the amplifier's individual stages differs from the theoretical tapered distributed amplifier, the optimization constraints ensure that the amplifier as a whole operates in a distributed manner and has a flat gain response.

As the optimizer was configured to minimize power consumption, the transistors are sized as large as possible given the bandwidth constraint, and their bias voltages are set such that the required gain is attained. For the given topology, this results in MOSFETs that are biased at the transition between strong inversion and velocity saturation, which comes at the cost of linearity performance. Linearity can be improved however, by simply increasing the biasing voltages. Naturally, this comes at the cost of an increased power consumption. Section 4.4 discusses the process of increasing the linearity of the prototype amplifier, while limiting the increase in power consumption.

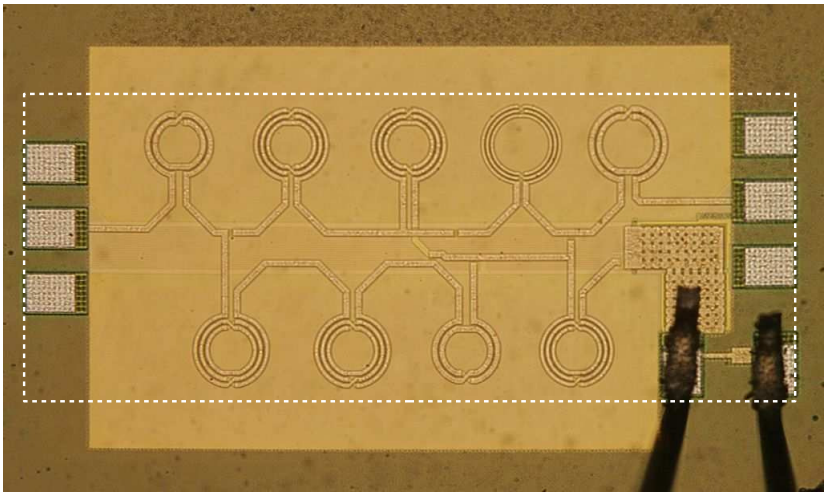


Figure 4.6: Micrograph of the tapered matrix amplifier. The occupied die size is 0.88 × 0.35 mm^2 (dashed line).

4.3 Experimental Results

Figure 4.6 shows a picture of the processed prototype amplifier. In this section, the measured performance of the prototype is presented and compared to the simulation results. The performance of the amplifier is also compared to the state of the art.

4.3.1 Measurement Setup

The die is mounted on a small PCB, the **probe board**, shown in Figure 4.7. The bias connections at the bottom-right of the die are wire-bonded to the probe board on which decoupling capacitors are placed. A header connector is soldered to the board to easily connect to the bias board discussed below. Also shown in Figure 4.7 are the probes which take care of connecting the large measurement equipment to the tiny integrated circuit.

Figure 4.8 shows the setup at the MICAS high-frequency measurement lab for measuring the prototype's small-signal performance. In this setup, the network analyzer needs to be placed behind the probe station to allow for tensionless connection with the probes. As this makes the controls of the network analyzer hard to reach, the latter is operated remotely using the keyboard, mouse and display on the left-hand side of the picture. The probe board is placed directly below the microscope on the probe station's chuck. The microscope is indispensable in precisely positioning and landing the probes on the probe pads of the die.

A custom-made **bias board**, powered from a single lab power supply, is used to generate the bias voltages for the amplifier using configurable resistive dividers and voltage buffers. The bias board also provides probe points for easily measuring the current drawn by the amplifier. The bias voltages are respectively fed to the network analyzer

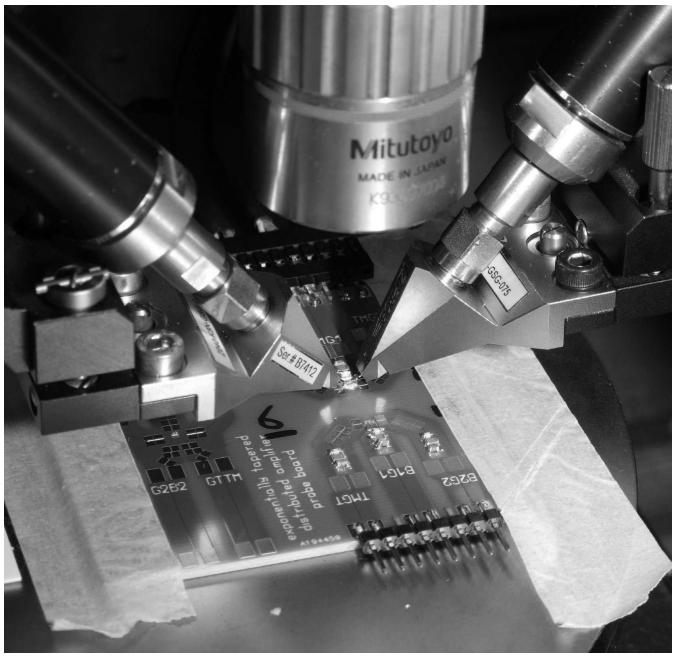


Figure 4.7: Probe board secured to the chuck. On the left and the right are the probes with the network analyzer's cables connected on top.

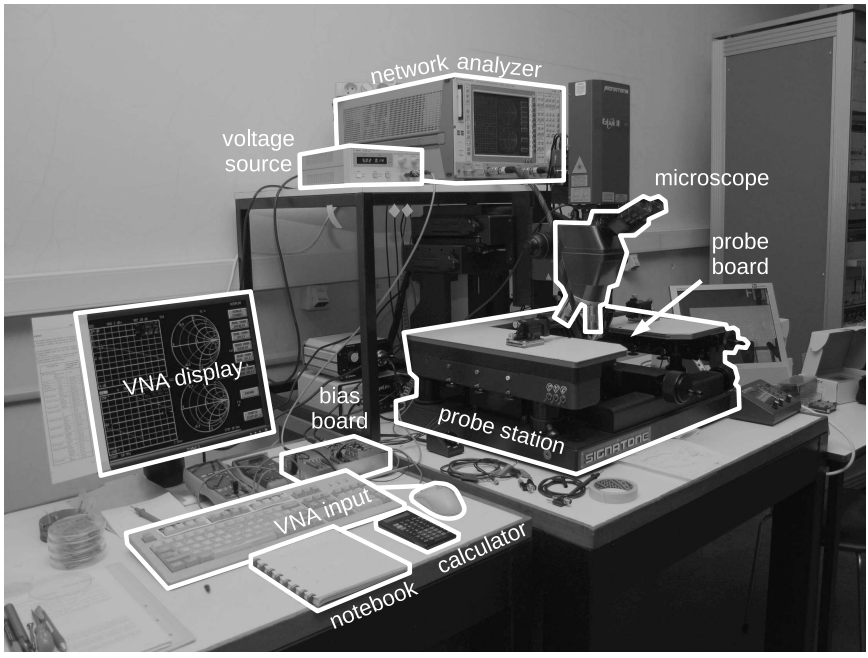


Figure 4.8: Small-signal measurement setup at the MICAS measurement lab.

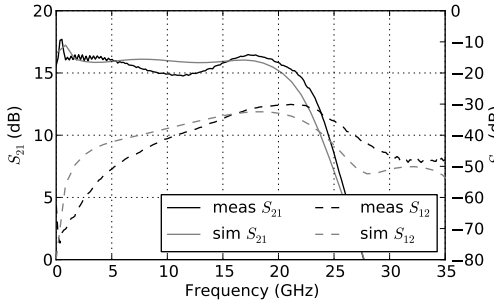


Figure 4.9: Forward and reverse gain measurements and simulation.

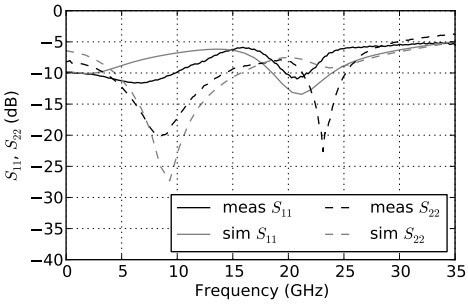


Figure 4.10: Reflection coefficients measurements and simulation.

and to the probe board.

For the linearity and noise measurements, the network analyzer is replaced with the appropriate equipment. The rest of the setup remains the same.

4.3.2 Small-Signal Properties

S-parameter measurements have been performed using the Agilent E8361C PNA network analyzer in combination with Cascade Microtech 110 GHz GSG Infinity probes with 75 µm pitch. The input and output LC ladders are biased through the PNA. The interstage ladder is biased through the bondwire visible in the bottom right of Figure 4.6.

All small-signal measurements agree well with the simulations, demonstrating the fidelity of the component models. Figure 4.9 plots the measured and simulated forward and reverse gain. S_{21} variation between three measured samples measured under the same biasing conditions is less than 0.5 dB. The mean gain in the 22 GHz pass-band is 15.8 dB, slightly less than the 16 dB simulated mean gain. The DC power consumption is at 12.86 mW also virtually identical to the simulations. The gain variation in the pass-band is about 1.5 dB. The peak around 500 MHz is due to the resonance between the bondwire and decoupling capacitor necessary for biasing the interstage LC ladder. Even though no cascode gain cells were used to reduce the feedback through C_{gd}, reverse isolation is adequate, exceeding 30 dB.

Input and output reflection coefficients are displayed in Figure 4.10. Maxima in the pass-band, -6 dB for S_{11} and -8 dB for S_{22} are relatively large for a distributed amplifier, owing to the intentional mismatching of the input transmission line and the output line tapering, as discussed in Sections 3.3.2 and 2.4.3 respectively. The µ stability factor, calculated from the S-parameters and shown in Figure 4.11, indicates that the amplifier is unconditionally stable across the frequency spectrum. Finally, the group delay variation shown in Figure 4.12 is 32 ps in the pass-band.

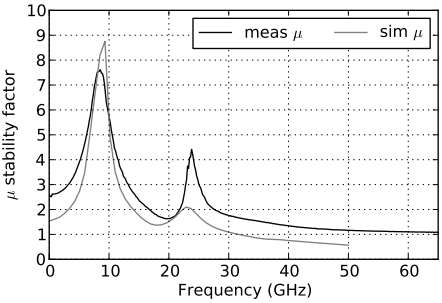


Figure 4.11: μ stability factor.

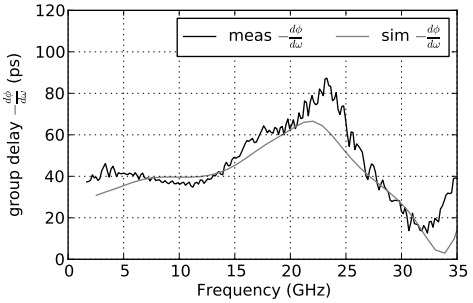


Figure 4.12: Group delay measurements and simulation.

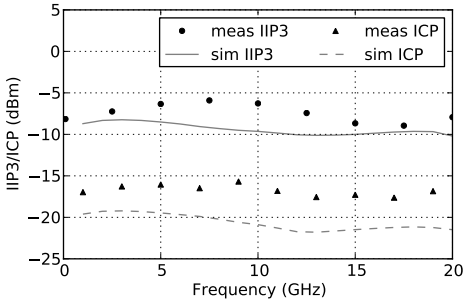


Figure 4.13: Measured versus simulated input-referred third-order intermodulation product (IIP3) and 1 dB compression point (ICP).

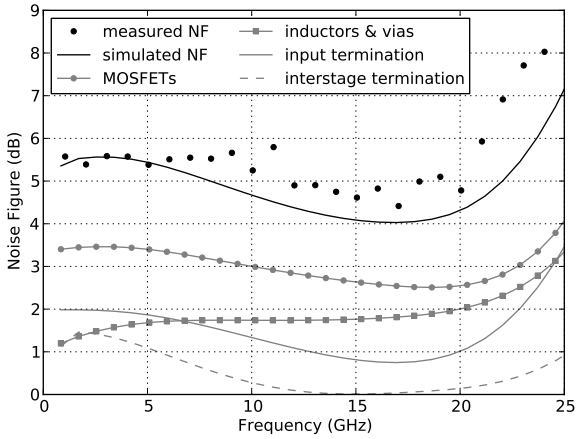


Figure 4.14: Measured versus simulated noise figure. The (simulated) contributions of the various noise sources in the circuit are plotted in gray.

4.3.3 Linearity

The input-referred third-order intercept (IIP3) and 1 dB compression point (ICP) measurements were performed using two Agilent E8357D signal generators and a R&S FSU spectrum analyzer. A R&S NVRS power meter with a NRV-Z52 thermal power sensor was used to determine the absolute available input power. The IP3 measurements were performed with 10 MHz tone spacing. The measured values for IIP3 and ICP are plotted, together with the simulations, in Figure 4.13. The plotted values are the effective input power levels, calculated from the available power by means of S_{11}.

4.3.4 Noise

Noise figure measurements were executed with the help of a R&S FSIQ26 spectrum analyzer with FS-K3 software and a NoiseCom NC346C switchable noise source. An Agilent 83051A pre-amplifier was inserted between the DUT and the spectrum analyzer. This setup was used to measure the global noise figure of everything after the noise source up to and including the spectrum analyzer. The NF from the DUT was subsequently calculated from this global NF by numerically removing the noise contributions of the other components in the setup: spectrum analyzer, cables, bias-T's, probes, adapters and the pre-amplifier. Insertion losses from these components have been extracted from data-sheets or measured with a R&S ZVM VNA. The details of the noise measurement are described in Section 4.3.4.1. The resulting NF is plotted in Figure 4.14, showing a minimum of 4.4 dB and a maximum of 6 dB.

The (simulated) contributions of the various noise sources in the circuit are also plotted in Figure 4.14. Each of the curves shows the noise figure of the amplifier due to only a single group of noise sources. The MOSFETs are the primary source of noise, in particular the MOSFETs in the first stage [Fri44]. The noise due to the termination resistors

show a similar frequency dependence as in a traditional distributed amplifier, peaking near DC. This suggests that these noise contributions can be reduced by increasing the number of gain cells in each stage [Ait85].

It is important to note that above 7 GHz, the noise generated by the inductors, interconnect and vias (to the MOSFETs) is the second largest contributor to the output noise, even approaching the MOSFET noise level and should therefore not be omitted in analytical noise models of the distributed amplifier. Previously published noise analyses [Ait85, Zha06, Hey07] neglect the thermal noise introduced by losses present in the inductors and interconnect. Design decisions based on these analytical noise transfer functions may therefore not necessarily lead to optimum noise performance when losses are considerable.

The noise performance can be improved by increasing the number of fingers of the transistors [Sch06]. Also the MOSFETs' biasing points can be optimized for noise performance. Both methods have the largest impact when applied to the transistors of the first stage [Fri44]. The two-stage design thus allows tuning the first stage for noise and the second stage for linearity, facilitating the design of a low-noise, high-linearity amplifier.

4.3.4.1 Noise Measurement Details

Noise measurements can be quite hard to get right. It is not simply a matter of connecting the DUT to the measurement equipment and pressing a button or two. One has to be well aware of exactly what steps are necessary to obtain an accurate measurement. Thankfully there are a number of excellent application notes from the measurement equipment industry. Agilent [Agib, Agic, Agia] and Anritsu [Anra, Anrb] have a number of very detailed application notes on measuring noise figures. From these documents, it is clear that quite a few corrections need to be performed in order to obtain a truthful value for the noise figure of a device. Another very good reference is a book by Thomas Lee [Lee04b], which contains an introduction to noise measurements.

The noise figure of the prototype amplifier was measured using a R&S FSIQ26 spectrum analyzer with FS-K3 noise measurement software and a switchable noise source. This setup basically performs a Y-factor measurement. As the noise figure of spectrum analyzers is typically large[7], it is necessary to insert a low-noise pre-amplifier, reducing the noise figure of the combination [Lee04b]. Even with the pre-amplifier in place, the measured noise figure still needs to be corrected using Friis' formula for the noise figure of cascaded devices [Fri44]. In addition, the losses present in everything but the DUT also affect the measured noise figure and their contributions need to be subtracted from the noise figure. The measurement setup is represented in Figure 4.15. Cables, bias-T's, probes, and coax conversion adapters all introduce losses that need to be removed from the net noise figure. All components except from the conversion adapters are included in Figure 4.15.

The FS-K3 software offers an operation mode (labeled *2nd stage correction*) that aims to assist in removing the contributions of components other than the DUT from the noise

[7] The noise figure of the FSIQ26 is about 15 to 20 dB [Sch00].

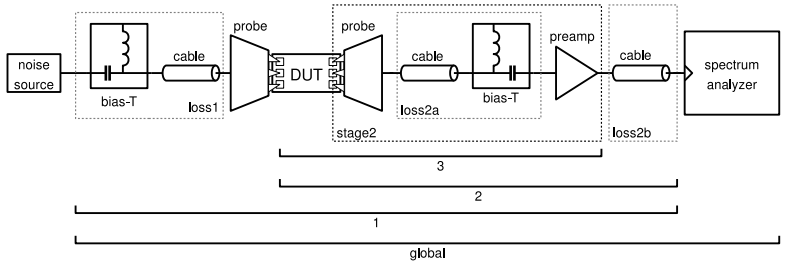


Figure 4.15: Schematic representation of the noise figure measurement setup. The indications *global*, *1*, *2* and *3* at the bottom correspond to the different steps in the de-embedding of the DUT's noise figure.

figure. Unfortunately, the manual [Sch00] is not entirely clear on what calculations are being performed under the hood. Therefore, the FS-K3 software was only used to obtain the noise figure for the total measurement setup and the DUT noise figure was manually de-embedded.

Starting from the noise figure of the complete measurement setup NF_{global}, we de-embed the noise figure of the DUT in a number of steps. In a first step, the noise contribution of the FSIQ26 is removed using Friis' formula for the noise figure of a cascade of noisy components [Fri44]:

$$F_{\text{cascade}} = F_{\text{first}} + \frac{F_{\text{second}} - 1}{G_{\text{first}}}, \tag{4.7}$$

where G_{first} is the *available gain* of the first stage. Note that (4.7) is in terms of the noise factor F, the noise figure in linear terms.

The noise factor of the part indicated by "1" in Figure 4.15 is then given by

$$F_1 = F_{\text{global}} - \frac{F_{\text{FSIQ26}} - 1}{G_{\text{global}}}, \tag{4.8}$$

where G_{global} is the available gain of the complete measurement setup. The spectrum analyzer measures the *transducer gain* (based on knowledge of the noise source's power output). The available gain can be calculated from the setup's S-parameters and the reflection coefficient of the noise source [Poz05], which have both been characterized manually using an R&S ZVM VNA.

To accurately characterize the losses associated with the cables and bias-Ts, the circuits indicated by *loss1*, *loss2a* and *loss2b* in Figure 4.15 have also been measured individually with the ZVM VNA. Losses associated with the probes and conversion adapters are provided by the manufacturers in data sheets. As the noise factor of a passive attenuator is equal to its attenuation [Fri44], (4.7) can be simplified if the first component is an attenuator:

$$F_{\text{cascade}} = \frac{1}{G_{\text{att}}} + \frac{F_{\text{second}} - 1}{G_{\text{att}}} \tag{4.9}$$

$$= \frac{F_{\text{second}}}{G_{\text{att}}}. \tag{4.10}$$

Applying (4.10), one can see that removing the noise contribution due to the **components in front of the DUT** (bias-T, cable and probe) simply involves multiplying the noise factor by the power gain of these components:

$$F_2 = F_1 \cdot \left|S_{21,\text{loss1}}\right|^2 \cdot \left|S_{21,\text{probe}}\right|^2. \tag{4.11}$$

The corresponding gain is also easily calculated:

$$G_2 = \frac{G_{\text{global}}}{\left|S_{21,\text{loss1}}\right|^2 \cdot \left|S_{21,\text{probe}}\right|^2}. \tag{4.12}$$

The noise contribution due to attenuation in the cable right before the spectrum analyzer can also be removed using (4.7):

$$F_3 = F_2 - \frac{1/\left|S_{21,\text{loss2b}}\right|^2 - 1}{G_3}, \tag{4.13}$$

with

$$G_3 = \frac{G_2}{\left|S_{21,\text{loss2b}}\right|^2}. \tag{4.14}$$

To remove the **second-stage contribution**, we first calculate the noise figure of *stage2* by applying (4.10) again:

$$F_{\text{stage2}} = \frac{F_{\text{preamp}}}{\left|S_{21,\text{probe}}\right|^2 \cdot \left|S_{21,\text{loss2a}}\right|^2}. \tag{4.15}$$

Finally, using (4.7) once again, the noise figure of the DUT can be determined:

$$F_{\text{DUT}} = F_3 - \frac{F_{\text{stage2}} - 1}{G_{\text{DUT}}}, \tag{4.16}$$

where G_{DUT} is the available gain of the DUT, calculated from the measured S-parameters. Figure 4.16 shows the result of the de-embedding method described above. Correcting for the attenuation of the components in front of the DUT, which exceed 3 dB at 20 GHz, has by far the largest contribution in the de-embedding process. The de-embedded noise figure agrees fairly well with the values predicted by the circuit simulator over the full measured spectrum. The increasing divergence from the simulated values and the jittery character of the measured data can be attributed to mismatches between components in the setup[8], as the de-embedding did not consider these. Thanks to the amplifier's high gain, the resulting error is small, but can be further reduced by also taking into account the reflection coefficients of the different stages when performing the calculations [Col02].

[8] Recall that the input impedance of the amplifier is close to 100 Ω.

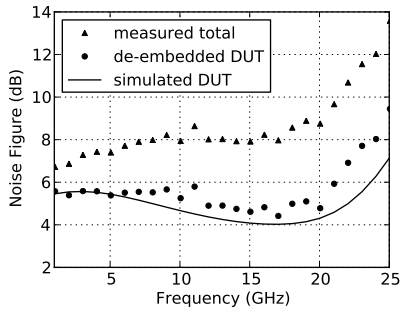


Figure 4.16: Plot showing the measured global noise figure of the measurement setup of Figure 4.15 and the de-embedded and simulated DUT noise figures.

4.3.5 Comparison with State of the Art

The performance measures of the amplifier are summarized in Table 4.1 together with those of other published broadband (low-noise) amplifiers featuring a comparable bandwidth. Alongside distributed amplifiers, also resistive-feedback amplifiers [Par06b, Che07, Che09, Oku09] and one inductively degenerated common-source amplifier with input filter [Bev04] are included in the table. The areas reported in the table include bond- and probe-pads.

The presented amplifier shows the highest gain-bandwidth product to power consumption ratio, validating the use of distributed amplifiers in low-power applications. To allow the amplifier to operate at frequencies down to DC, the biasing currents flow through the termination resistors of the input and interstage LC ladders. Sacrificing amplification near DC, coupling capacitors can be inserted to further reduce the power consumption by 35 %, to 8.5 mW, making the amplifier even more competitive.

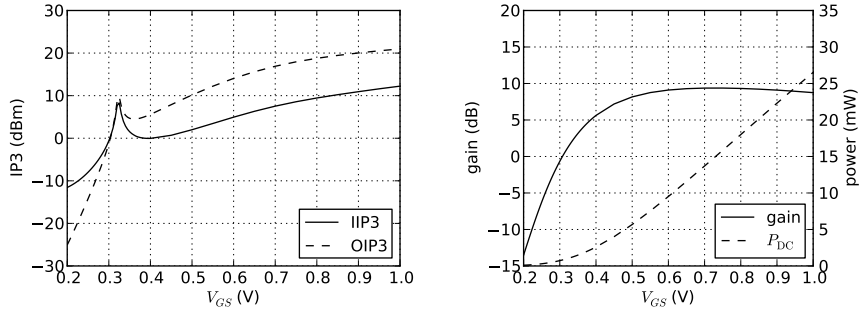
Even without optimizing the noise performance of the amplifier, the noise figure is still comparable to those of the low-noise amplifiers in the table. The amplifier's noise figure can be further reduced by optimization, making the TMA suitable for low-noise applications. The focus on low-power and the high gain of the amplifier does come at the cost of linearity performance, however. Nonetheless, when comparing the prototype to amplifiers featuring a similar linearity [Bev04, Par06b], the prototype shows much higher gain and bandwidth and at the same time occupies a much smaller die area, illustrating the advantages of the tapered matrix amplifier. Additionally, in Section 4.4, we demonstrate that only slight changes to the design can significantly improve the linearity of the prototype.

The used die area is among the smallest in the table. Only a resistive-feedback amplifier [Oku09] is smaller, but it's gain is 5 dB lower, showing the topology's inherent gain-bandwidth limitation. Also, it is not clear whether the power dissipation of the output buffer is included in the 8.4 mW reported for this amplifier. Furthermore, we believe that the area of the presented TMA could be reduced by about 30 %, to approximately 0.2 mm^2, by arranging the inductors in staggered lines.

Table 4.1: Broadband (Low-Noise) Amplifier Performance Comparison

	CMOS [µm]	**flat-gain BW [GHz]**	**avg S_{21} [dB]**	**spot NF [dB]**	**IIP3 [dBm]**	**ICP [dBm]**	**P_{DC} [mW]**	**Area [mm^2]**
This Work	0.09	0 – 22	15.8	4.4 - 6	-8.9 – -5.7	-17.6 – -15.7	12.9	0.31
[Zha06]	0.18	0 – 6.2	8.1	4.2 – 6.2	3 at 2 GHz	-8.5	9	1.16
[Par06b]	SiGe 0.18	0.2 – 10	11	2.9 – 3.3	-7.8 – -5*	-17.5 – -14.5*	9.6	0.88
[Che07]	0.18	2 – 11.5	12	3.1 – 4.0	3 at 5.5 GHz	-8.5 at 5 GHz	13.4	0.33
[Che09]	0.09	0.1 – 20	12	3.3 - 5.6	-4 – -1		12.6 + 7.8 (buf)	0.35
[Oku09]	0.09	0 – 22.5	10.7	4.3 – 6.5†	-6.1 – -2.7		8.4 + ?	0.13
[Hey07]	SiGe 0.18	0 – 12	8.5	2.9 – 4	-4.1 – -3.0	-12.2 at 9GHz	21.6	0.76
[Chi07] (3x3)	0.18	0 – 31	16.7			- 8.3	260	2.3
[Moe08]	0.13	3 – 9.4	12.1	1.8 – 4.7		-9 – -5	30	0.83
[Liu04]	0.18	0 – 22	7.5	4.3 – 6.1‡	8.7	- 2	52	1.35
[Tsa04]	0.18	0 – 23	9		-1 at 10 GHz	-9.5 at 10 GHz	60	0.36
[Bev04] (TW)	0.18	2.9 – 8.7	10	4.2 – 6.2	-10.8 – -8	-18 at 6 GHz	9 + 9 (buf)	1.1

∗ from 3 to 10 GHz † from 0 to 15 GHz ‡ from 0 to 18 GHz



(a) (b)

Figure 4.17: NMOS with $W = 16 \times 2$ µm, $L = 80$ nm, $V_{DS} = 1.2$ V at 10 GHz: (a) third-order intercept point, and (b) gain and power consumption.

4.4 Linearity-Enhanced Design

Overall, the prototype amplifier's performance is very competitive with amplifiers featuring a similar bandwidth. However, the low-power design strategy does come at the cost of linearity performance, reflected in the relatively low IIP3 and ICP values in Table 4.1. In this section, the prototype design is revisited with the aim at improving the linearity of the amplifier.

Linearity of the MOSFETs is strongly related to the chosen biasing point. As a MOSFET's transconductance g_m approaches a constant value in velocity saturation (Figure 3.17b), linearity performance improves with increased overdrive voltages [Lee04a, San06]. Illustrating this, Figure 4.17a shows the third-order intercept point (IP3) of a single NMOS transistor as a function of the gate-source bias. Since the bias voltages of the prototype amplifier are fairly low, the linearity performance of the amplifier can be easily improved by driving the transistors further into saturation. However, this comes at the cost of a steeply increased power consumption, as is apparent from Figure 4.17b.

Alternatively, MOSFETs show a "sweet spot" in the third-order intercept point for a particular overdrive voltage [Too04]. However, this sweet spot is located in moderate inversion, where the gain of the MOSFET is very low. Biasing the MOSFETs at the sweet spot, requires placing more MOSFETs in parallel to obtain an adequate total gain. For the prototype amplifier, increasing the number of parallel gain cells is very difficult due to the combination of the line tapering and increased characteristic impedance. Also, it would increase the die area significantly. For these reasons, the sweet spot biasing is not considered here.

Another method to reduce distortion in an amplifier is to employ negative feedback [Raz01]. Source-degeneration is one way to easily introduce negative feedback into the prototype amplifier. However, negative feedback also reduces the gain of the amplifier.

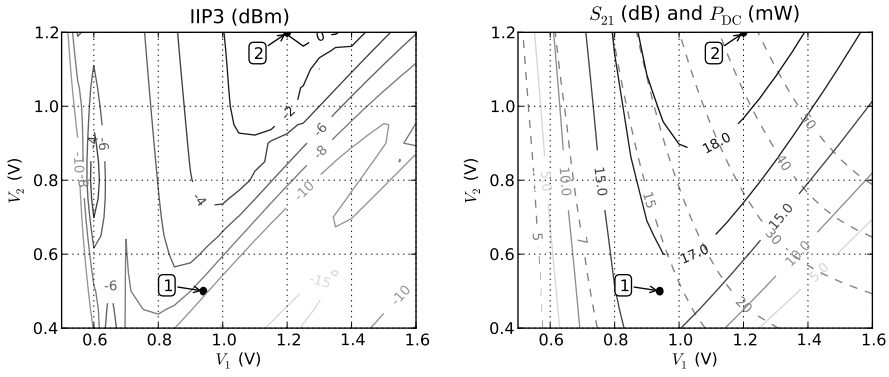


Figure 4.18: Contour plot of the amplifier's specifications at 10 GHz as a function of the second-stage bias voltages V_1 and V_2; (a) input-referred 3rd order compression point in dBm, and (b) gain in dB (solid) and DC power consumption in mW (dashed). The circuit's original low-power bias point (1) and an alternative bias-point (2) showing good linearity performance, but also high power consumption, are indicated.

4.4.1 Design Procedure

In this section, we investigate the use of higher bias voltages and degeneration resistors to increase the amplifier's linearity, while limiting the increase in power consumption. In a first step, the bias voltages to the transistors are increased changed to boost the linearity of the amplifier. In a second step, degeneration resistors are inserted to reduce the power consumption.

4.4.1.1 Increasing the Bias Voltages

As the signal amplitudes are the largest in the second stage of the amplifier, distortion first occurs at the output. Therefore, it makes sense to increase only the voltages V_1 and V_2 biasing the second-stage transistors (M3 and M4 in Figure 4.5). Figure 4.18a shows the effect on the circuit's operation when altering V_1 and V_2. Increasing both to 1.2 V increases the IIP3 to 0 dBm, an improvement of 10 dB. Note that altering V_1 and V_2 does not disturb the distributed operation of the amplifier, as the relative amplitudes of the output currents of M3 and M4 do not change. This implies that it is possible to adjust V_1 and V_2 as a function of the required gain or linearity in a reconfigurable receiver system.

On a side note, Figure 4.17a also shows the IP3 sweet spot around $V_1 = 0.6$V, with a maximum IIP3 of about -3 dBm (hard to see in the figure). The corresponding bias point reduces the gain to 5 dB, illustrating that this is indeed not an option for the prototype amplifier topology.

Changing the bias points for M3 and M4 does not only affect the amplifier's linearity, but also its gain and power consumption. Figure 4.18b shows that the suggested bias

point increases the power consumption to 46 mW, nearly four times the original design's 12.6 mW. However, the alternative bias-point also increases the gain by 3 dB to 18.6 dB. This extra gain can be sacrificed in order to reduce the amplifier's power consumption.

4.4.1.2 Reducing the Power Consumption

In order to moderate the power consumption, degeneration resistors can be inserted at the sources of transistors M3 and M4. However, this is not the only option; the width of M3 and M4 can be reduced to the same end. Alternatively, downsizing and degeneration can be combined. This methodology agrees with the distortion-aware design guidelines by Baki et al. [Bak06], to bias small, degenerated transistors at the highest possible overdrive voltage where g_m distortion is minimized. In a power-aware design, the overdrive voltage needs to be limited however, as g_m/I efficiency drastically drops with increasing V_{GS}. While Baki et al. do not explicitly make this point, the sample LNA design demonstrating their recommendations is in fact biased at a relatively low gate-source voltage, ensuring good g_m/I efficiency.

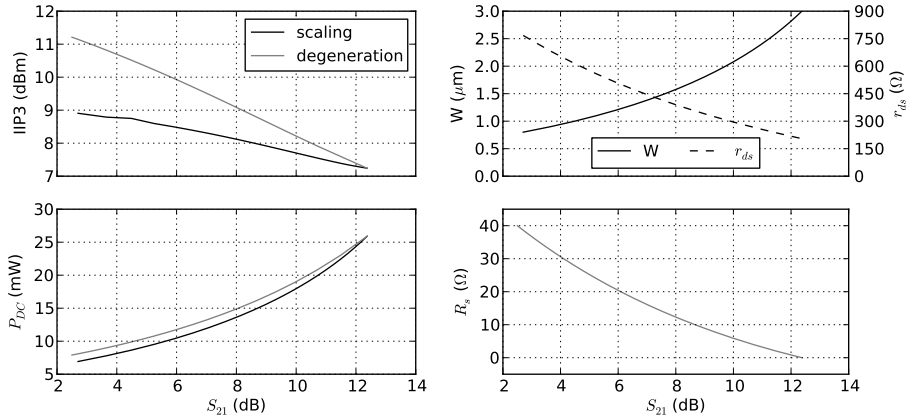
Baki et al. recommend both using a small transistor and adding a degeneration impedance. However, transistor sizing and source-degeneration affect distortion in different ways, but it is not clear in what proportion. Transistor sizing affects distortion in a number of ways [Bak06]. Distortion due to the transconductance g_m is independent of the transistor sizing. Distortion due to the parasitic capacitances C_{ds} and C_{gd} decreases with transistor size but the effect is fairly weak. Similarly, distortion due to the output resistance r_{ds} is less for smaller transistors (larger r_{ds}). The exact decrease of the harmonic components depends on the initial transistor size and biasing.

The effect of a degeneration resistor on distortion is more straightforward. The second-order and third-order distortion are inversely proportional to respectively the square and the cube of the degeneration resistance value. A degeneration resistor is therefore expected to have a larger effect on reducing distortion than scaling down the transistor.

Illustrating the effects of transistor scaling versus resistive degeneration, Figure 4.19a plots an NMOS transistor's IIP3 and power consumption as a function of the gain. For the same gain, the power consumption is nearly identical for both techniques. It is clear that source degeneration offers a significant advantage over transistor downsizing. Degeneration allows increasing the IIP3 by approximately 1 dB for each 3 dB drop in gain versus only 0.5 dB per 3 dB for downsizing; degeneration is the better choice when one wants to exchange gain for linearity performance. Figure 4.19b shows the required transistor width and degeneration resistance to obtain a given gain. Additionally, it shows the output resistance r_o of the scaled transistor. The parasitic capacitances C_{ds} and C_{gd} are simply proportional to the transistor width and are therefor not shown.

Figure 4.20 shows the same plots for the amplifier of Figure 4.5 with $V_1 = V_2 =$ 1.2 V. The figure compares the performance of the amplifier in which the second-stage transistors are scaled[9] or degenerated. The plots show a close resemblance to those of the single-transistor case. For example, the power consumption for the same gain is nearly identical for the two techniques and degeneration allows for a larger increase

[9] Additional capacitance is added so that the total capacitance at the nodes of M3 and M4 is unaltered.



(a) (b)

Figure 4.19: (a) Effect of transistor scaling versus resistive degeneration of a single NMOS transistor on its IIP3 and power consumption, and (b) required scaling factor and degeneration resistance as a function of the gain.

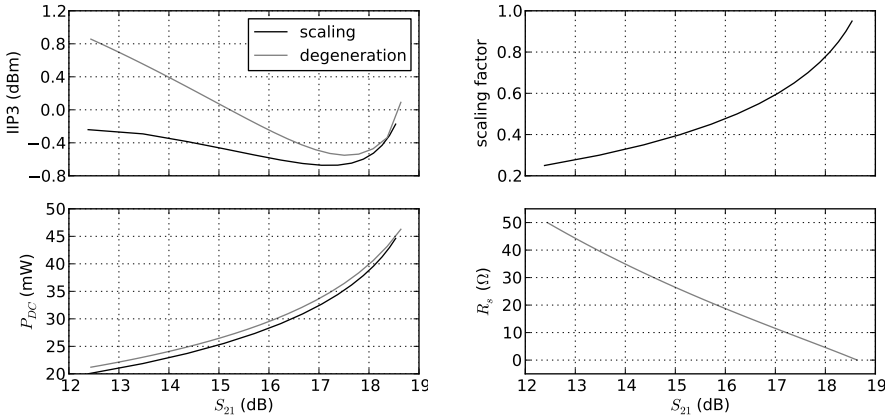
of the IIP3. In contrast, for small departures from the initial configuration (where the gain is approximately 17.5 dB), the IIP3 drops slightly, which is not the case for the single-transistor case. Nevertheless, the power consumption of the amplifier can be considerably reduced while retaining its linearity performance.

To reduce distortion as much as possible, we opt to maintain the transistor sizes and insert degeneration resistors. From Figure 4.20, employing degeneration resistors of 30 Ω reduces the gain to 14.6 dB, only slightly less than the 15.8 dB of the original design, but it brings the power consumption down to 25.4 mW. The IIP3 is 0.2 dBm, a 10 dB improvement over that of the original design. This presents a good compromise between power consumption and linearity performance and is the configuration selected for further analysis.

Due to the fact that the amplifier's operation deviates from that of an ideal distributed amplifier, the introduction of degeneration resistors in the second-stage transistors disturbs the flat response. To restore the flat gain response, the components (MOSFET sizes and resistances) are optimized , as was detailed in Section 4.2.1. The optimized component values are shown in Figure 4.21. Additionally, to improve the noise performance of the amplifier, the number of fingers in the first-stage transistors M1 and M2 are increased, as suggested in Section 4.3.4. The performance of the amplifier is discussed and compared to that of the original design in the next section.

4.4.2 Simulation Results

Figure 4.22 compares the forward and reverse gain of the original and linearity-enhanced amplifier design. The enhanced design sacrifices some gain in order to allow for good linearity performance at relatively low power consumption. The circuit optimization



(a) (b)

Figure 4.20: (a) Effect of transistor scaling versus resistive degeneration of M3 and M4 on the prototype amplifier's (with $V_1 = V_2 = 1.2$ V) IIP3 and power consumption, and (b) required scaling factor and degeneration resistance of M3 and M4 as a function of the gain.

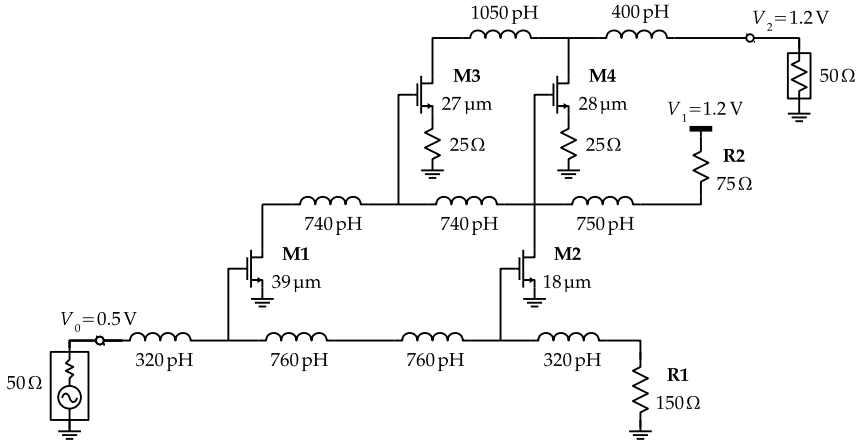


Figure 4.21: Linearity-enhanced tapered matrix amplifier. In order to restore the flat gain response after insertion of the degeneration resistors, the transistor sizes and termination resistances have been adjusted.

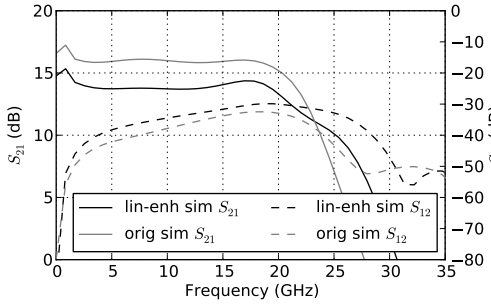


Figure 4.22: Forward and reverse gain of the linearity-enhanced design.

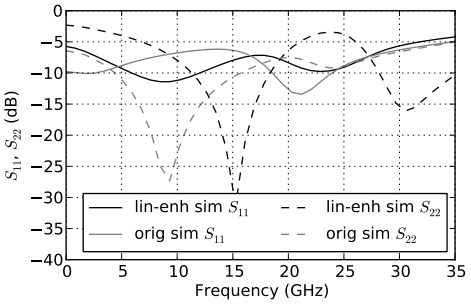


Figure 4.23: Reflection coefficients of the linearity-enhanced design.

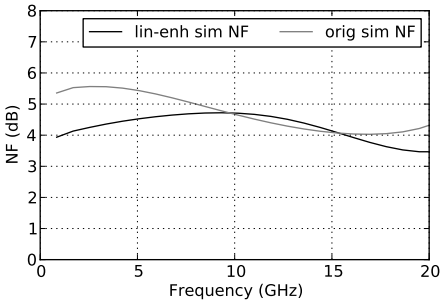


Figure 4.24: Noise figure of the linearity-enhanced design.

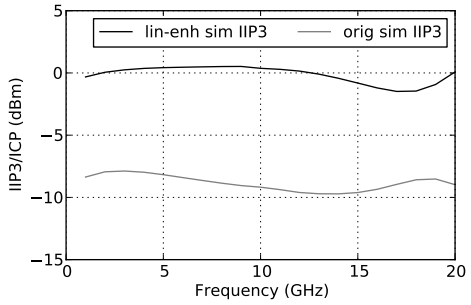


Figure 4.25: Input-referred IP3 of the linearity-enhanced design.

ensured that the gain response remains flat. Reverse isolation is slightly reduced compared to the original design, but is still good. The levels of the input and output reflection coefficients of the presented amplifier, shown in Figure 4.23, are comparable to those of the original design.

The noise figure, with an average of 4.26 dB, is shown in Figure 4.24. The average noise figure is about 0.5 dB lower compared to that of the original design. This is mostly due to increasing the number of fingers of the first-stage transistors M1 and M2. Without this change, the average noise figure of the linearity-enhanced design is about the same as before.

Input-referred third-order intercept simulations are shown in Figure 4.25. The new design shows a 10 dB improvement in IIP3 across the pass-band. The average simulated IIP3 is 0 dBm. The input-referred 1-dB compression point also shows an improvement of 10 dB (not plotted) over the original design. The good agreement between the simulation and measurement results of the original design gives confidence that the simulations of the linearity-enhanced design accurately predict its performance. As the IIP3 simulations of the original design underestimated the measured IIP3 values (by up to 4 dB), it is expected that the actual average IIP3 of the enhanced design will be about 3 dBm.

As the inductors have not been altered from the original design, the IC area has not changed. The two extra degeneration resistors are placed alongside the MOSFETs and do not require extra die area.

Table 4.2 summarizes the performance of the linearity-enhanced distributed LNA design and that of amplifiers featuring a similar bandwidth. The new design demonstrates one of the highest IIP3 values while still offering a high gain. The power consumption of 21.7 mW is very low for an amplifier featuring the given gain, bandwidth and linearity performance.

4.5 Conclusion

The ideas presented in Chapter 3 have been combined in the design of a low-power two-stage tapered matrix amplifier in a 90 nm CMOS technology. Target specifications for gain and bandwidth were set to 15 dB and 20 GHz, respectively. Aiming to minimize power consumption as much as possible, the characteristic impedance of the tapered transmission line sections should be increased. Due to the inherent limitations in the characteristic impedance that is attainable, the number of sections of each amplifier stage is limited to two. The 2×2 tapered matrix amplifier topology is mutated by inserting an extra section–but no gain cell–into the input and interstage transmission line, allowing for larger transistors.

As the individual stages consist of only two sections, the new tapering scheme presented in Chapter 3 cannot be used, unfortunately. Since the use of the conventional tapering scheme requires the addition of extra capacitance, limiting the characteristic impedance, it is preferably avoided. In the tapered matrix amplifier, however, the frequency response of the individual stages does not necessarily need to be flat, providing an extra degree of freedom in the design. In addition, the non-perfect approximation of the transmission lines with LC ladders, losses in the inductors and FETs and the gate-drain feedback capacitance make that the amplifier's operation differs significantly from the theory. Therefore, the extra capacitance is omitted and it is left to a circuit optimizer to try and obtain a flat frequency response in a pragmatic design approach.

The initial size of the transistors is determined from the bandwidth requirement, and based on a simple expression for the topology's gain, the transistors' initial biasing conditions are determined. The optimizer is allowed to change the MOSFET sizes, inductor geometry, the values of the termination resistors and the bias voltages on the three LC ladders. One constraint makes sure that the amplifier operates in a distributed fashion, requiring equal phase delays between two gain cells in each stage. Others constraints make sure the gain and bandwidth specifications are met. Finally, optimization goals enforce a flat gain response and minimize the power consumption.

Measurements of the amplifier show good agreement with simulations. The amplifier shows a 22 GHz flat-band gain of 15.8 dB and a very low power consumption of 12.9 mW. Compared to amplifiers featuring a similar bandwidth, both distributed and other topologies, it shows a record gain-bandwidth-to-power consumption ratio. Even though some resistive-feedback amplifiers manage to obtain a bandwidth of 20 GHz, they fail to produce a high gain. Also the occupied die area of 0.31 mm^2, although not as small as

Table 4.2: Broadband (Low-Noise) Amplifier Performance Comparison for the Linearity-enhanced Prototype.

	CMOS [µm]	**flat-gain BW [GHz]**	**avg S_{21} [dB]**	**spot NF [dB]**	**IIP3 [dBm]**	**ICP [dBm]**	**P_{DC} [mW]**	**Area [mm^2]**
lin-enhanced (sim)	0.09	0 – 20	14.0	3.5 – 4.7	-1.5 – 0.5	-13.2 – -10.3	21.7	0.31
original (sim)	0.09	0 – 20	16.0	4.0 – 5.6	-9.7 – -7.9	-21.79 – -19.22	12.8	0.31
original (meas)	0.09	0 – 22	15.8	4.4 – 6	-8.9 – -5.7	-17.6 – -15.7	12.9	0.31
[Zha06]	0.18	0 – 6.2	8.1	4.2 – 6.2	3 at 2 GHz	-8.5	9	1.16
[Par06b]	SiGe 0.18	0.2 – 10	11	2.9 – 3.3	-7.8 – -5*	-17.5 – -14.5*	9.6	0.88
[Che07]	0.18	2 – 11.5	12	3.1 – 4.0	3 at 5.5 GHz	-8.5 at 5 GHz	13.4	0.33
[Che09]	0.09	0.1 – 20	12	3.3 - 5.6	-4 – -1		12.6 + 7.8 (buf)	0.35
[Oku09]	0.09	0 – 22.5	10.7	4.3 – 6.5†	-6.1 – -2.7		8.4 + ?	0.13
[Hey07]	SiGe 0.18	0 – 12	8.5	2.9 – 4	-4.1 – -3.0	-12.2 at 9GHz	21.6	0.76
[Chi07] (3x3)	0.18	0 – 31	16.7			- 8.3	260	2.3
[Moe08]	0.13	3 – 9.4	12.1	1.8 – 4.7		-9 – -5	30	0.83
[Liu04]	0.18	0 – 22	7.5	4.3 – 6.1‡	8.7	- 2	52	1.35
[Tsa04]	0.18	0 – 23	9		-1 at 10 GHz	-9.5 at 10 GHz	60	0.36
[Bev04] (TW)	0.18	2.9 – 8.7	10	4.2 – 6.2	-10.8 – -8	-18 at 6 GHz	9 + 9 (buf)	1.1

$*$ from 3 to 10 GHz † from 0 to 15 GHz ‡ from 0 to 18 GHz

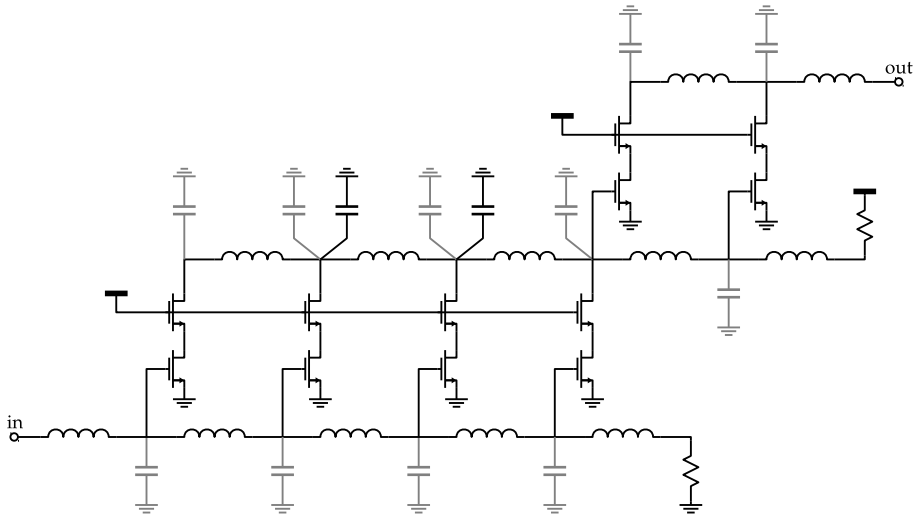


Figure 4.26: The basic circuit configuration of the first prototype.

the smallest resistive-feedback amplifier, still is among the lowest in its class, illustrating that the distributed amplifier is an economically viable option. Even though the noise figure was not specifically considered in the design, the average noise figure of 5.4 dB holds up well with other broadband low-noise amplifiers. In addition, simulations show that the noise figure can be reduced by 0.5 dB by employing more fingers in the layout of the MOSFETs. Some of the low-power design choices did lead to a relatively low linearity; at an average of -7.3 dBm, the input-referred third-order compression point is among the lowest. The high gain of the amplifier is partly responsible for the low IIP3, as the output-referred compression point is better ranked.

The design was revisited in an attempt to improve the linearity of the amplifier. As the bias voltages used in the design were fairly low, linearity can be easily improved by increasing the overdrive voltage of the second-stage transistors, but at the cost of a steeply increased power consumption. However, the increased bias voltages also boost the gain. This extra gain headroom is subsequently sacrificed to reduce the power consumption through the introduction of degeneration resistors. Simulations of the final linearity-enhanced design show an improvement in the IIP3 of 10 dB to about 0 dBm, at a moderate increase of the power consumption to 22 mW, less than double of the original design. The gain is reduced to 14 dB, which is still high compared to what is achieved by the other amplifier topologies. The enhanced design illustrates that the tapered matrix amplifier is capable of highly-linear, low-noise amplification, at a high gain and low power consumption.

4.6 The Story of a Misadventure

The prototype amplifier (design 2) discussed in this chapter was not the first amplifier to be designed in the context of this research project. It was preceded by another amplifier

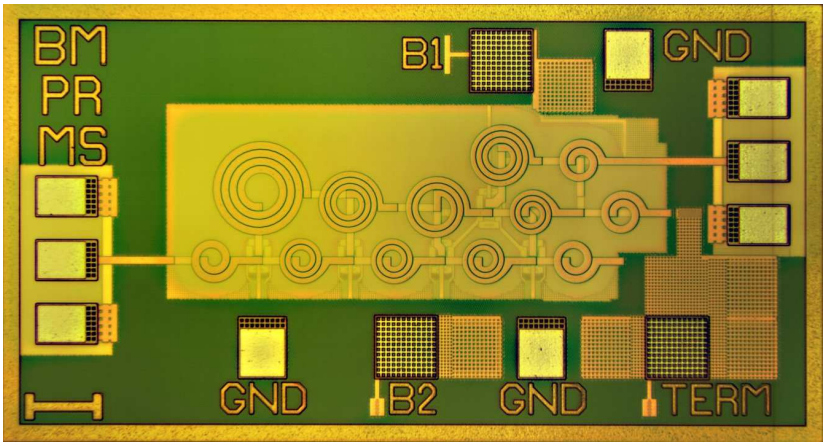


Figure 4.27: Micrograph of the first prototype. The occupied die size is 0.9×0.46 mm^2
.

(design 1) with similar specifications. Unfortunately, the measurements of the latter did not agree well with the simulations. The circuit of this amplifier is shown in Figure 4.26 and the die is shown in Figure 4.27. In this section, the differences with the second design are briefly discussed and its performance is evaluated.

There are a number of notable differences between the two amplifier designs:

- The first design is not really a tapered matrix amplifier, but rather a cascade of a 4-section and a 2-section tapered distributed amplifier.
- The first stage is a 4-section distributed amplifier
- Cascode gain cells were used, improving reverse isolation, but also requiring two extra bias voltages.
- The placement of the inductors mimics the circuit structure and therefore the ground is distributed using thin strips passing underneath the inductors. Additionally, a wide ground conductor surrounds the circuit to improve the distribution of the ground. This complicates the layout and is not very area-efficient, as can be seen in Figure 4.27.

The design of the first amplifier relied less on optimization. As there were no inductor macro-models available at the time of the design, only the transistors, resistors and capacitors were optimized[10]. The inductor geometry was chosen manually, based on the first-order circuit model, and modeled using ADS Momentum.

The specifications (from simulation) of the first amplifier are close to those of the second design: a 16 dB flat gain across a 20 GHz bandwidth. The power consumption of 30 mW is much higher than that of the second design. The linearity is somewhat better though,

[10]Optimization of the transistors resulted in the omission of the second stage's right gain cell.

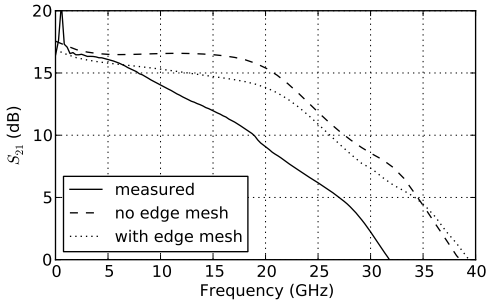


Figure 4.28: The first prototype's measured forward gain versus simulations with and without edge mesh in the inductors.

showing an IIP3 of around -6 dBm. The average noise figure of 5.8 dB is worse. Finally, the die area of 0.41 mm^2 is slightly larger than that of the second prototype.

As mentioned above, measurements of the latter did not agree well with the simulations. The exact cause of the discrepancy between the measurements and simulation was not discovered. However, an important error in the inductor models was identified. When simulating structures in a field solver, correct meshing is paramount in obtaining valid results [Swa03]. In simulating the complete structure encompassing the 12 inductors and the ground frame/lines, it was left to Momentum to automatically perform edge meshing. While an edge mesh was correctly generated in the surrounding ground frame, alas, this was not the case for the inductor windings. Practically, this results in an underestimation of signal attenuation due to skin-effect losses. The difference between the amplifier's gain with (manual edge mesh setting) and without edge-meshing in the inductors is shown in Figure 4.28. The amplifier's measured gain is also plotted. While the missing edge mesh cannot explain the full discrepancy with the measurements, it is responsible for a significant drop in gain at the high end of the pass band.

In retrospect, some important lessons were learned that helped in the design of the second prototype:

- The availability of inductor macro-models enables optimizing the inductor geometry, providing more means to optimize all specifications of the amplifier.
- Arrangement of the inductors in two rows significantly simplifies the layout of the amplifier and provides a much better ground connection.
- One should verify that the output of the field solver is correct. The availability of inductor models in the design kit enables validation of EM simulations.

Chapter 5

Traveling-Wave Transistor

The bandwidth of a distributed amplifier is typically limited by the cut-off frequency of the artificial transmission lines connecting the gain cells, as discussed in Section 2.1. For a given characteristic impedance, the cut-off frequency of an LC ladder is determined by the transistor's parasitic capacitance value. For distributed amplifiers employing planar transmission lines, the cut-off frequency is determined by the transistors' parasitic capacitance and their spacing. In general, the bandwidth is thus determined by the size of the individual gain cells; by reducing the size of the gain cells, the bandwidth can be increased. One can imagine making the gain cells infinitesimally small and placing them very close together. In the limit, a continuous distributed amplifier is obtained, which is essentially a very wide FET. The gate and drain of this FET form transmission lines coupled by a distributed transconductance, expressed in Siemens per meter. Operation of the continuous distributed amplifier is identical to that of the lumped version. However, as the bandwidth limitation due to the lumped capacitances has been removed, the bandwidth of the amplifier is only limited by the electron transit time. On the other hand, this continuous distributed amplifier still suffers from the same limitation present in its lumped brother; due to losses present in the gate and drain lines, it is not possible to increase the gain of the amplifier indefinitely by increasing its width.

It was discovered that the wide FET structure can also support a different mode of operation, supporting an exponentially growing wave. In this mode, the device acts like an active transmission line and its gain could be increased indefinitely simply by increasing its width. The prospect of a device capable of exciting an exponentially growing wave showed a lot of promise and generated quite some interest among researchers. In the next section, the long history of the traveling-wave transistor is summarized, highlighting the discovery of the exponentially growing mode. Next, the operating principle of the growing mode is investigated with the help of transmission-line models. Using these models, the design of a traveling-wave FET in CMOS is investigated in Section 5.3. Finally, the stability of the traveling-wave transistor is analyzed.

5.1 History of the Traveling-Wave Transistor

This section attempts to provide a comprehensive overview of the publications on the traveling-wave transistor since the term was first coined in 1965. The discussion focuses on the traveling-wave transistor capable of supporting a growing wave. Key insights into the operation of the device and the different models are highlighted. In literature, a number of different names have been used to refer to the two operating modes of the

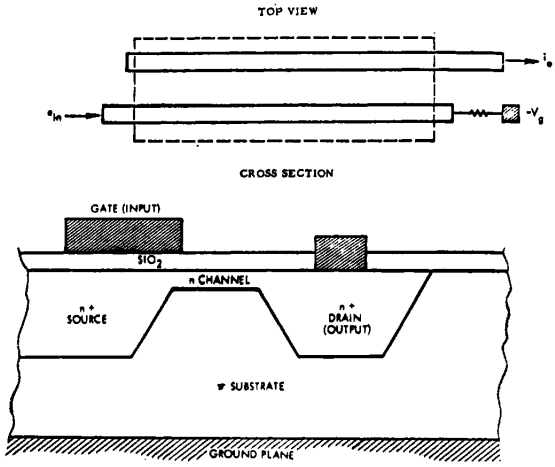


Figure 5.1: The traveling-wave transistor described by McIver [McI65].

traveling-wave transistor. In this chapter, the term *traveling-wave FET* (or *traveling-wave transistor*) is used to refer to both types of devices. The term *distributed FET* is used to indicate the traveling-wave FET that operates analogous to the distributed amplifier and *growing-wave FET* is used to designate the traveling-wave FET capable of supporting an exponentially growing wave.

In 1965, McIver first suggested the idea of a continuous distributed amplifier [McI65]. The input and output terminals of the device are strip-type transmission lines linked by an active FET, continuously distributed along the length of the lines (Figure 5.1). The device is modeled by means of a differential equation, neglecting losses and passive coupling between input and output lines. In order to obtain a flat-band gain response, the phase velocities of the input and output lines must be equal, as is the case in a lumped distributed amplifier. Similarly, the lines need to be properly terminated to avoid reflections. The only frequency dependence is due to the transconductance, determined by the overlap of the gate over the channel (gate-to-channel capacitance) and channel conductivity.

Kopp analyzed the traveling-wave transistor using coupled-mode theory [Kop66], where unidirectional waves are assumed. The latter implies a matched termination of the lines. Like McIver, Kopp also neglects losses and passive coupling, only including the non-reciprocal transconductive coupling between the lines.

Jutzi [Jut68] was the first to take capacitive coupling between the gate and drain lines into account. Reasoning that capacitive coupling is more significant than inductive coupling in devices such as tubes and transistors, inductive coupling is neglected. The three-conductor uniform transmission line is modeled by means of 2x2 per-unit-length impedance and admittance matrices, as depicted in Figure 5.2. The solution to the second-order differential transmission line equation is a superposition of decoupled fast (even) and slow (odd) wave modes, exhibiting different characteristic impedances. In the slow mode, the additional distributed loading due to the active and passive coupling

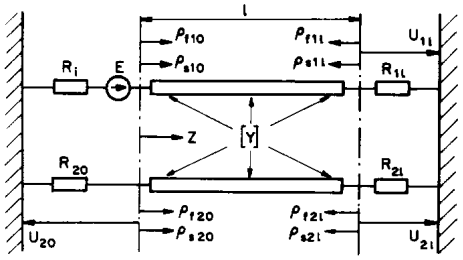


Figure 5.2: Modeling of the uniform distributed FET using per-unit-length impedance and admittance matrices [Jut68].

is negative, allowing negative attenuation. For sufficiently long lines, only the amplified slow mode must be considered and an expression for the gain of the device is derived, showing exponential gain. Stability is mentioned in passing, but is not investigated.

Kohn and Landauer provide a physical background on Jutzi's analysis of the traveling-wave FET, clearly illustrating the importance of passive coupling [Koh68]. Introduction of C_{dg} coupling (with zero g_m) gives rise to the existence of two modes of propagation: the fast (even) and the slow (odd) mode. In the slow mode, a non-zero transconductance generates a source-drain current which is out of phase with the source-drain voltage and thus acts as a negative resistance. It is this effect that causes exponential signal growth. Since the exponential gain is made possible through C_{dg}, the effect is frequency-dependent and the feedback path disappears at low frequencies. The feedback also causes peaking at high frequencies, possibly leading to instabilities or oscillations. Finally, it is stated that the existence of the growing mode is not dependent on phase velocity synchronization between the gate and drain lines. Supporting the discussion, measurements of a lumped distributed amplifier using tubes are shown. On increasing C_{dg}, the measurements show exponentially growing oscillations, shown in Figure 5.3.

More than ten years later, Podgorski and Wei presented a slightly more complex traveling-wave transistor model that includes losses [Pod82]. However, passive coupling between the gate and drain lines is not included, and the growing mode is therefore not investigated. For the conventional distributed amplifier mode, it is shown that the gain increases with transistor width up to an optimum width. This is analogous to the number of gain cells in a lumped classic distributed amplifier after which the gain decreases again due to losses [Bey84] (see Section 2.2).

Wei C-J. proposed the use of an image gate in a distributed FET to achieve phase velocity synchronization [Wei83]. Although the gate-drain capacitance is included in the model, focus is again on the classic distributed amplifier operation.

In 1984, Holden and Oxley presented a unified traveling-wave FET model, including capacitive but excluding inductive coupling, valid for both types of traveling-wave transistors; the so-called traveling-wave or distributed amplifier (TWA) and the traveling-wave FET (TWF) capable of supporting a growing wave mode [Hol84]. A full four-conductor coupled line modal analysis using per-unit-length Z and Y matrices is performed. The TWF has two lossy modes and one exponentially growing mode, while the TWA has

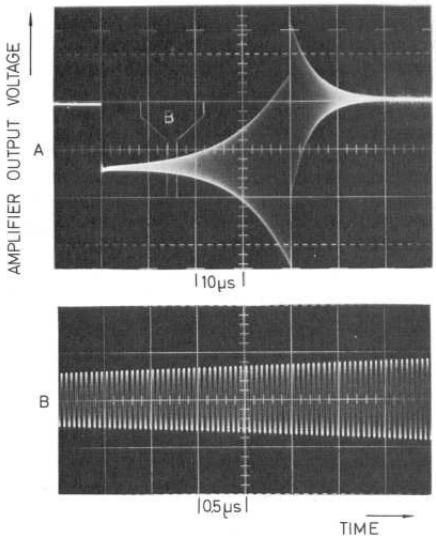


Figure 5.3: Measurements showing the exponentially growing wave in a lumped growing-wave FET prototype [Koh68]

only lossy modes. It is interesting to see that the gain in the TWA can be expressed in terms of the two lossy modes. The model shows that a 2 mm TWA can provide more gain than a 2 mm TWF due to the former's higher characteristic impedance. While the TWF gain increases with increased width, the usable width is limited because the reciprocal nature of the device and mismatched boundaries cause "Fabry-Perot" oscillations leading to instabilities. Holden and Oxley disagree with Kohn, stating that phase velocity synchronization is necessary for both traveling-wave FET types but that they merely achieve this in different ways.

The next year, Holden et al. report about a prototype GaAs TWF making use of the exponentially growing wave mode [Hol85]. In this TWF, periodically positioned overlay capacitors on the drain line have been used to balance the waves on the gate and drain

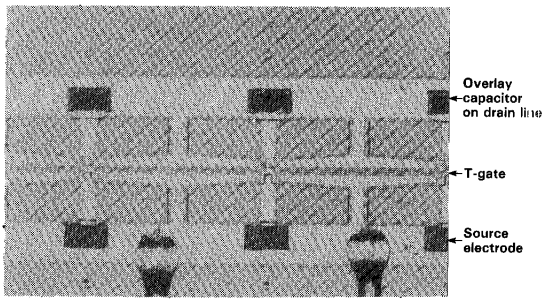


Figure 5.4: In the "traveling-wave FET" by Holden et al., the source and drain electrodes are spaced far apart to increase the inductive reactance [Hol85]

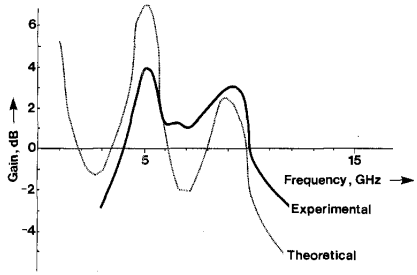
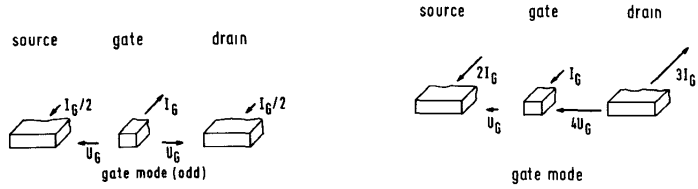


Figure 5.5: The gain of a 3-mm-wide TWT shows sharp "Fabry-Perot" peaks, indicating traveling-wave action with mismatched boundaries [Hol85]

lines. The presence of this capacitance has a dramatic effect on the eigenmodes of the device and is responsible for producing the strong growing mode. Additionally, a T-shaped gate is used to reduce the series resistance of the 3 mm wide gate. The device is modeled by means of a passive multicoupled transmission line model based on per-unit-length impedance and admittance matrices. The model is completed by adding an active admittance matrix to the passive admittance matrix. The dominance of the inductive reactance over the line resistance, achieved by spacing the drain and source electrodes far apart, as shown in Figure 5.4, is claimed to be essential for the existence of the growing mode. The growing mode is said to be due to the feedback effect of the mutual inductance between drain and gate, which compensates for the high loss of the gate line. It is necessary to properly feed the device and terminate its terminals such as to excite the growing mode and suppress the lossy modes. Measurements of the prototype GaAs TWF show the "Fabry-Perot" peaks typical of a mismatched reciprocal device, visible in Figure 5.5.

As operating frequencies increase, the wavelength approaches transistor dimensions and traditional device models may prove inadequate. A journal paper by Heinrich and Hartnagel presents a rigorous full-wave analysis of wave propagation along MESFET electrodes in order to assess the impact of traveling-wave effects [Hei87b]. The presented model is the most complete model so far, including both inductive and capacitive coupling, losses and small-signal amplification. A mode-matching technique reveals the existence of three modes: gate (Figure 5.6), drain and bulk mode. For the usual FET structures, all modes are lossy, not capable of giving rise to a growing wave. Only by altering the device structure, a growing mode can be supported, for example by using a T-shaped gate [Hol85] or by providing positive feedback from the drain to the gate. However, Heinrich and Hartnagel warn that, because of the non-directionality of the device, growing waves could lead to severe instabilities if not properly matched. Alternatively, the FET structure could be made such that losses are reduced but no growing waves exist.

In 1998, Sebati et al. presented measurements of a continuous traveling-wave transistor operating like the classic distributed amplifier [Seb89]. The device uses a T-gate to reduce the gate resistance. In order to synchronize the phase velocity, the drain is loaded with a distributed Schottky diode.



(a) (b)

Figure 5.6: The gate mode for (a) zero and (b) non-zero transconductance [Hei87b]

Han et al. performed a small-signal transient analysis of a GaAs distributed amplifier [Han90]. It is shown that the presence of C_{gd} necessitates coupled-mode analysis, revealing fast and slow wave modes. C_{gd} also causes considerable dispersion, making it impossible to obtain a broad-band match. Furthermore, when the capacitive coupling between the two lines is significant, one mode shows a negative attenuation constant, leading to the exponential gain (growing-wave FET). However, this is not necessary to obtain gain (distributed FET).

Farina et al. [Far94] performed a similar full-wave analysis as Heinrich and Hartnagel [Hei87b], confirming that regular FET structures cannot support a growing mode. In 1995, they apply their theory to a FET with a T-gate [Far95]. The existence of the growing mode is explained by means of Poynting's theorem. Some design criteria are given for obtaining a structure supporting a growing mode. One of these states that phase-velocity synchronization between gate and drain lines is required. Also, asymmetric devices should be better suited for obtaining a growing mode.

In 1997, Farina et al., extend the model originally presented in 1994 [Far97b, Far97a]. Necessary prerequisites and topological aspects relevant to the existence of growing modes are discussed. The modes are calculated from a distributed equivalent-circuit model, and the effect of the different components in the circuit are discussed. This discussion is in a way similar to that of Kohn and Landauer [Koh68], but the growing mode is explained in terms of Poynting's theorem instead of negative resistance. Requirements include minimization of ohmic losses and maximization of feedback fields between the gate and drain. Important in obtaining the growing mode is asymmetry of the device; more specifically, the gate-source capacitance should be larger than the gate-drain capacitance. Another interesting conclusion is that capacitive and inductive coupling are mutually conflicting. For predominant capacitive coupling, the slow mode is the growing mode, as had already been shown before [Jut68, Koh68]. In a traveling-wave FET where inductive coupling is dominant, the fastest mode is the growing mode. Simulation results of a growing-wave amplifier using discrete FETs are also given, showing the gain as a function of the feedback capacitance C_{gd} (Figure 5.7). Feeding and termination are also mentioned. The authors also warn that, because the device is reciprocal, any deviation from a perfect match causes severe instability problems.

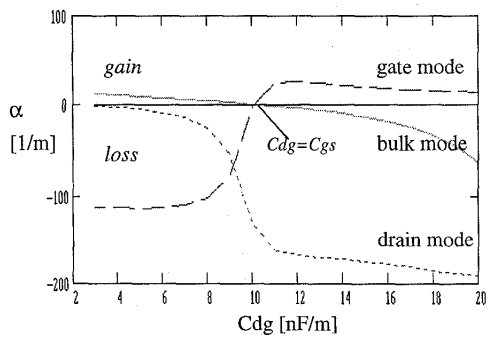


Figure 5.7: Attenuation constant versus feedback capacitance C_{gd} for the different wave modes [Far97b]

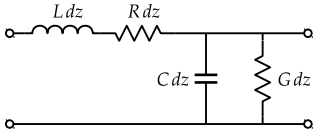


Figure 5.8: Equivalent circuit of an infinitesimal two-conductor transmission line section

5.2 Modeling the Growing-Wave FET

As is clear from the many publications, the traveling-wave FET can be analyzed in a multitude of ways. Still, even after more than forty years and dozens of publications on the subject, it remains somewhat vague how one can design a traveling-wave FET supporting a growing mode.

In this section, the requirement for obtaining a growing mode is intuitively discussed by means of the simple two-conductor transmission-line model. The insights developed from that model are then applied to a more complex three-conductor transmission line model capable of modeling a traveling-wave transistor.

5.2.1 Simple Active Transmission Line Model

One way of looking at the growing-wave FET is in terms of an active transmission line. The simple uniform two-conductor transmission line equivalent circuit model is shown in Figure 5.8. The wave equation for this transmission line is [Col01]

$$\frac{d^2}{dz^2}V(z) = (R + j\omega L)(G + j\omega C)V(z) \tag{5.1}$$

The solution to this wave equation describing the voltage waves on this transmission line is expressed by

$$V = V^+ e^{-\gamma z} + V^- e^{\gamma z} \tag{5.2}$$

where γ is the propagation constant, expressing the relation between the voltages at two different points along the transmission line:

$$\begin{aligned}\gamma &= \sqrt{(R+j\omega L)(G+j\omega C)} \\ &= \sqrt{(RG-\omega^2 LC)+j\omega\,(LG+RC)}.\end{aligned} \tag{5.3}$$

The propagation constant is a complex number of which the real part is the attenuation constant α, and the imaginary part is the phase constant β. The characteristic impedance links the voltages to the currents at any point on the line and is given by [Poz05]

$$Z_0 = \sqrt{\frac{R+j\omega L}{G+j\omega C}} = \frac{V^+}{I^+} = -\frac{V^-}{I^-}. \tag{5.4}$$

The average transmission line one encounters in everyday life is typically of a passive nature, reflected in a positive attenuation constant. In contrast, the growing mode in a traveling-wave FET originates from a negative attenuation constant [Lee04a]. An expression for the attenuation constant can be derived from (5.3):

$$\alpha = Re\{\gamma\} = \sqrt{0.5\left[\sqrt{\omega^4\,(LC)^2+\omega^2\,[(LC)^2+(RC)^2]+(RG)^2}+(RG-\omega^2 LC)\right]} \tag{5.5}$$

While (5.5) is exact, the complex square root in (5.3) is a multiple-valued function and α can thus be positive or negative. As passive transmission lines cannot support growing modes, it is obvious that α is positive. When any of R, L, G or C is negative however, α can be negative, but that is not apparent from (5.5).

Assuming low losses ($R \ll \omega L$ and $G \ll \omega C$), the RG term in (5.3) can be neglected. The first two terms of the binomial series expansion of (5.3) then provide an approximation for the propagation constant [Col01]:

$$\gamma \approx \frac{1}{2}\sqrt{LC}\left(\frac{R}{L}+\frac{G}{C}\right)+j\omega\sqrt{LC} \tag{5.6}$$

The expression for the characteristic impedance can be simplified under the same low-loss assumption:

$$Z_0 \approx \sqrt{\frac{L}{C}}+j\frac{\sqrt{LC}}{2\omega}\left(\frac{R}{L}-\frac{G}{C}\right) \tag{5.7}$$

The real part of (5.7) is not affected by the signs of R and G. For increasing frequencies, the imaginary part of (5.7) approaches zero and the expression reduces to the well-known result $\sqrt{\frac{L}{C}}$ in the high-frequency limit. The real part of (5.6) provides a simple expression for the attenuation constant as a function of the distributed elements. Furthermore, it also unveils the condition for obtaining a growing wave or a negative attenuation constant:

$$\frac{R}{L}+\frac{G}{C} < 0 \tag{5.8}$$

If we want to create an active transmission line by means of a negative shunt resistance, its value should be

$$-G > \frac{R}{L}C \approx \frac{R}{Z_0^2}. \tag{5.9}$$

This simple relation expresses, as could in fact be predicted by intuition, that the negative conductance should at least compensate for the series losses (relative to the characteristic impedance) in order to obtain a growing mode. This is one of the reasons why it is difficult to design a traveling-wave FET structure supporting a growing wave. As the thin gate of a FET is very lossy, the series losses represented by R are typically very large. T-shaped gates offer the same gate length but significantly reduce the gate series resistance, significantly facilitating the construction of traveling-wave FETs supporting growing-waves, as discussed in Section 5.1. Additionally, the simple model supports Holden's claim that the dominance of the inductive reactance over the line resistance is essential to the appearance of this growing mode [Hol85], as for a given capacitance C, the ratio of the inductance L to the resistance R should be as large as possible in order to minimize the right-hand side of (5.9).

Finally, it is interesting to note that the exponent of the gain expression derived for the three-conductor traveling-wave FET by Jutzi in his 1968 paper [Jut68] is identical to the expression for α (5.6) with $G = -\frac{1}{2}g_m$, substantiating the relevance of this simple active transmission line model.

5.2.2 Three-Conductor Transmission Line Model

As the FET is a four-terminal device, a traveling-wave FET should ideally be modeled as a four-conductor transmission line, complicating the analysis significantly. However, the basic findings of the preceding section can be transferred to the domain of multi-conductor transmission lines, as is shown in this section.

Multiconductor transmission lines (MTL) can be analyzed by means of modal decomposition (eigenanalysis). The eigenvalues and eigenvectors represent the propagation constants and voltage/current distributions of the modes [Pau08, Far93]. The characteristic impedances for the modes can be calculated from the propagation constants and eigenvectors. In the case of the traveling-wave FET, one (or possibly more) of these modes can be growing modes (having a negative attenuation constant). To build a device featuring an exponentially growing gain, the growing mode needs to be stimulated: terminating the FET using the mode's characteristic impedance and driving the device according to its eigenvector.

If the source of the FET is left floating, the traveling-wave FET has three eigenmodes [Hol84, Hol85, Hei86, Hei87b, Hei87a, Far94, Far95, Far97b, Far97a]. On the other hand, if the bulk and source are connected along the width of the FET, the device has only two eigenmodes and can be modeled as a three-conductor transmission line [Jut68, Hei83, Han90]. A homogeneous three-conductor traveling-wave FET can be modeled by 2×2 per-unit-length impedance and admittance matrices. The passive impedance

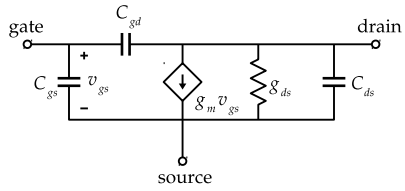


Figure 5.9: Small-signal circuit model for the FET transistor

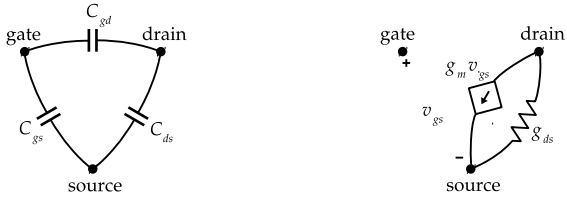


Figure 5.10: Schematic transmission-line cross-section for determining the (a) capacitance matrix and (b) conductance matrix.

matrix represents the series losses and inductance [Pau08]:

$$\mathbf{Z} = \mathbf{R} + j\omega\mathbf{L} = \begin{bmatrix} r_{11} & r_{12} \\ r_{21} & r_{22} \end{bmatrix} + j\omega \begin{bmatrix} l_{11} & l_{12} \\ l_{21} & l_{22} \end{bmatrix} \tag{5.10}$$

The admittance matrix can be seen as the sum of a passive admittance matrix $\mathbf{Y}'$ and an active admittance matrix $\mathbf{Y}''$ [Hol84, Hol85]. $\mathbf{Y}'$ is simply the per-unit-length admittance matrix of the passive FET, representing shunt losses and capacitance and $\mathbf{Y}''$ models the active part of the FET, the transconductance. The conductance and capacitance matrices can be readily derived from the small-signal FET model shown in Figure 5.9. Figure 5.10 shows the distributed cross-sectional transmission-line elements used to determine the admittance matrix

$$\mathbf{Y} = \mathbf{G} + j\omega\mathbf{C} = \begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix} + j\omega \begin{bmatrix} c_{11} & c_{12} \\ c_{21} & c_{22} \end{bmatrix} \tag{5.11}$$

The capacitance matrix is purely passive and given by

$$\mathbf{C} = \begin{bmatrix} C_{gs} + C_{gd} & -C_{gd} \\ -C_{gd} & C_{ds} + C_{gd} \end{bmatrix} \tag{5.12}$$

The conductance matrix models the transistor's transconductance g_m and output impedance $r_{ds} = 1/g_{ds}$:

$$\mathbf{G} = \begin{bmatrix} 0 & 0 \\ g_m & g_{ds} \end{bmatrix} \tag{5.13}$$

The asymmetry of G and positive off-diagonal element g_m indicate active non-reciprocal coupling. The coupled wave equations for a multi-conductor transmission line are given

by [Pau08]

$$\frac{d^2}{dz^2}V = \mathbf{ZY}V \tag{5.14}$$

$$\frac{d^2}{dz^2}I = \mathbf{YZ}I \tag{5.15}$$

These equations can be decoupled by diagonalizing the **ZY** and **YZ** matrices by means of a similarity transformation (eigendecomposition):

$$\mathbf{ZY} = \mathbf{T}\Lambda\mathbf{T}^{-1} \tag{5.16}$$

The diagonal elements of Λ are the eigenvalues or the square of the propagation constants of the decoupled modes and the matrix T holds the corresponding eigenvectors. Due to the need for eigendecomposition of **ZY**, the link between the per-unit-length components and the growing mode is not as easy to demonstrate as for the two-conductor transmission line. However, it is clear that some sort of negative impedance or admittance is required to obtain a growing mode. A negative resistance can be created by using a FET in the circuit configuration shown in Figure 5.11 [Raz01]. This circuit is typically used in oscillator circuits such as the Colpitts oscillator. The small-signal impedance seen between the gate and drain terminals of the FET is given by

$$Z_{\text{in}} = -\frac{g_m}{\omega^2 C_{gs} C_{ds}} + \frac{1}{j\omega C_{eq}} \tag{5.17}$$

where C_{eq} is the series combination of C_{gs} and C_{ds}. The real part of (5.17) is negative. Note that the absolute value of the resistance is frequency-dependent. The gain provided by the growing mode is therefore expected not to be flat as in the classic distributed amplifier.

Let's look at the conductance matrix for a negative conductance $-g_{gd}$ between the gate and drain conductors, as shown in Figure 5.12:

$$\mathbf{G} = \begin{bmatrix} 0 & g_{gd} \\ g_{gd} & 0 \end{bmatrix} \tag{5.18}$$

Comparing (5.18) to (5.13), the negative impedance due to the transconductance is thus not fully equivalent to a negative impedance. A negative impedance between gate and drain conductors provides reciprocal coupling whereas the transconductance provides only coupling from gate to drain. This is why the presence of the transconductance alone is not enough to cause the growing mode. If no coupling from drain back to the gate is present, the gate signal can not be regenerated and eventually fades out. Thus, for a growing mode to exist, coupling from the drain back to the gate line is required. This coupling can be inductive, capacitive, or resistive and passive or active.

When the gate and the drain lines are mutually coupled, modal decomposition reveals even and odd modes. In the even mode, there is no voltage between gate and drain lines and the negative resistance is effectively short-circuited; the mode is lossy. In the odd mode, there is a voltage over the negative resistance, giving rise to the growing mode.

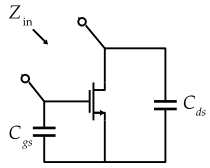


Figure 5.11: Negative resistance circuit

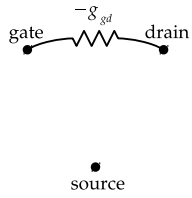


Figure 5.12: Transmission line cross-section with negative resistance between gate and drain conductors

In summary, to obtain a growing mode in a three-conductor – two signal conductors and a reference conductor – transmission line, there needs to be coupling from one signal conductor to the other and vice versa, of which at least one is active. The active coupling should be large enough to at least compensate the series and shunt losses of the passive structure, similar to what is described in Section 5.2.1.

5.2.3 Growing Waves and the Poynting Vector

In this section, we briefly look at the analysis of the growing-wave FET in terms of electromagnetic fields. More specifically, the distributed FET can be analyzed using Poynting's theorem [Far97a]. Poynting's theorem expresses the conservation of energy for electric and magnetic fields [Col01]. The real part of the complex Poynting theorem states that the time-averaged power that is dissipated (or generated) inside a volume V equals the amount of power that enters (leaves) this volume through its surface S:

$$Re\left\{\frac{1}{2}\oint_S \vec{E}\times\vec{H}^*\cdot\left(-d\vec{S}\right)\right\} = \frac{1}{2}\int_V \vec{E}\cdot\vec{J}^* dV, \tag{5.19}$$

where $\vec{E}$ and $\vec{H}$ represent the complex electric and magnetic field vectors and $\vec{J}$ is the current density. When the right-hand side of (5.19) is positive, power is dissipated in the volume. For a wave traveling along a transmission line, this means the wave loses power; the line is lossy. The sign of the term inside the volume integral is determined by the angle between the electric field vector $\vec{E}$ and that of the current density vector $\vec{J}$:

$$\vec{E}\cdot\vec{J}^* = ||\vec{E}||\cdot||\vec{J}^*||\cos\left(\vec{E},\vec{J}^*\right). \tag{5.20}$$

To obtain a growing mode, it is required that (5.20) is negative; $\vec{J}$ should have a component in the direction opposite of $\vec{E}$. This implies that the current flows from a low to a high electric potential. In circuit theory, a negative resistance models this effect.

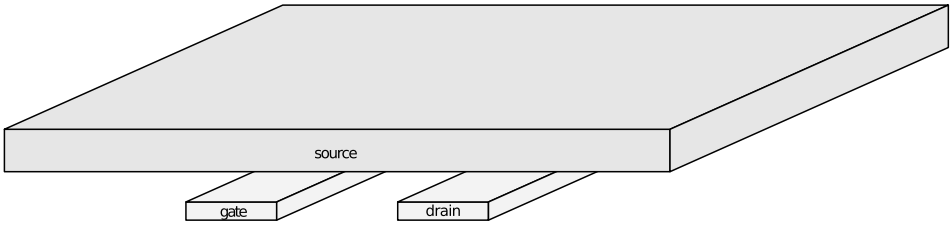


Figure 5.13: Gate-drain-source inverted microstrip line.

Applying Poynting's theorem to the growing-wave FET, the transconductance generates a channel current that is out of phase with the electric field. However, $\vec{J}$ contains, in addition to the transconductance current, also a conduction current due to ohmic losses in the channel. The transconductance current should thus first compensate for the ohmic losses present in the channel to be able to generate exponentially growing waves. In addition, the transconductance current should also compensate for the transmission line losses outside of the channel.

5.3 Design of a Growing-wave Amplifier in CMOS

As the gate resistivity of a MOSFET is very large and there is no option to alter the shape of the gate in a standard CMOS process, the feasibility of a continuous traveling-wave MOSFET is implausible. However, as has been demonstrated in the literature, a lumped implementation of the growing-wave FET is also possible, allowing for more design freedom.

In the following section, the design of a lumped growing-wave amplifier in a 130 nm standard CMOS technology is discussed. Due to difficulties in obtaining a growing mode in this amplifier, an alternative topology is presented in a second section.

5.3.1 A Lumped Growing-Wave Amplifier

To keep the design as simple as possible, the growing-wave amplifier is designed as a three-conductor transmission line; the bulk of each MOSFET is connected to its source. From the literature and the analysis in Section 5.2.1, we identify two important requirements for obtaining a growing mode: low loss and dominance of capacitive coupling over inductive coupling. In order to minimize losses, wide metal strips are used for the gate and drain lines. The source line serves as the reference conductor for the gate and drain lines in an upside-down microstrip configuration, shown in Figure 5.13. The lumped MOSFETs are placed between the gate and drain lines, their gates perpendicular to the transmission line, as shown in Figure 5.14. This allows having a large number of MOSFETs per unit length and increases the gate to drain line spacing, reducing inductive coupling.

A unit slice of the passive gate-drain-source transmission line can be simulated in an EM solver such as Sonnet em or Agilent ADS Momentum. An example of a unit slice is shown in Figure 5.15, where the ports are indicated by numbers from 1 to 8. Next

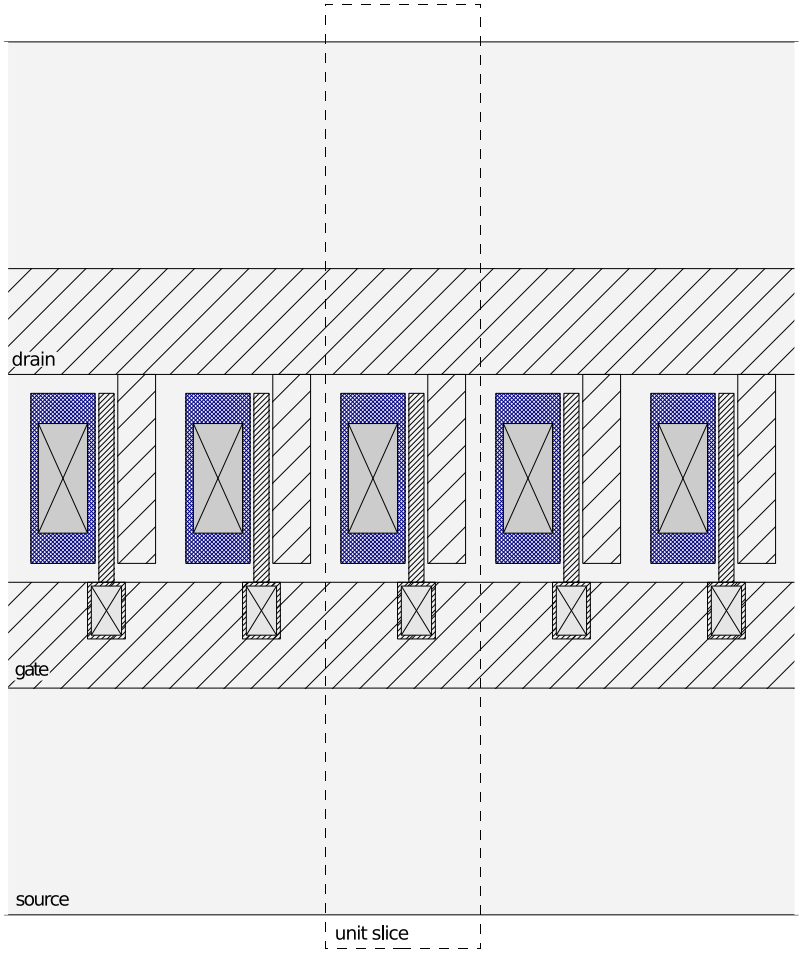


Figure 5.14: Layout of the lumped traveling-wave FET

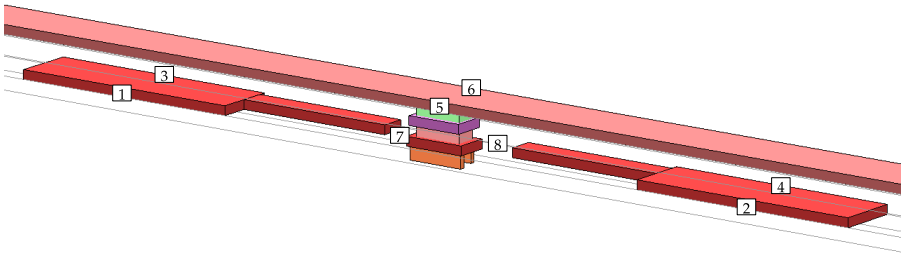


Figure 5.15: Slice of a lumped growing-wave FET amplifier in Sonnet em. The MOSFET model is plugged in at ports 7 (gate-source) and 8 (drain-source).

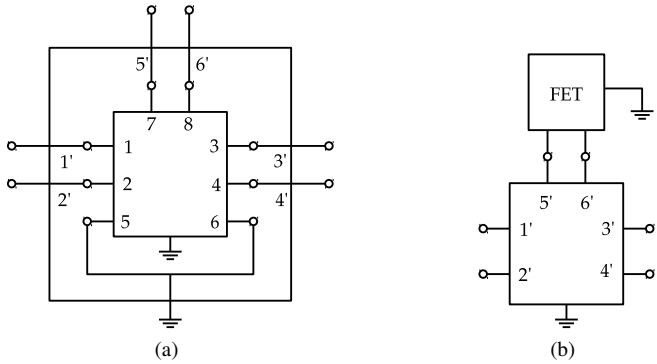


Figure 5.16: (a) Reduction of the 8-port output data from Sonnet into a 6-port model, and (b) Combination of the latter with the 2-port FET model.

to the six wave ports for the gate (1 & 3), drain (2 & 4) and source (5 & 6) lines, two internal ports (7 & 8) are configured where the intrinsic MOSFET model can be plugged in. The resulting 8-port S-parameter data is reduced to 6-port data by setting ports 5 and 6 (the source line) as a reference for ports 1 & 3 (gate) and 2 & 4 (drain), respectively, as depicted in Figure 5.16a. This 6-port S-parameter model is then, as is shown in Figure 5.16b, combined with a 2-port S-parameter model derived from the intrinsic (BSIM) MOSFET model provided by the CMOS foundry, yielding an accurate frequency-dependent 4-port model[1]. By performing modal analysis on this 4-port data, the existence of a growing mode can be investigated.

As the simulated structure is not uniform, it cannot be represented by per-unit-length Z and Y matrices. Nonetheless, modal decomposition can also be applied to non-uniform lines. Instead of diagonalizing the **ZY** matrix using eigendecomposition, the **A**, **B**, **C** and **D** matrices representing the $2n$-port are diagonalized [Far04]. The derivations made by Faria [Far04] assume the non-uniform multiconductor transmission line is reciprocally coupled, however. Due to the presence of the transconductance, this assumption is not valid for the traveling-wave FET, and thus it is necessary to alter the calculations for the general case, as detailed in Appendix B. Provided the line is approximately uniform, it is also possible to calculate approximate per-unit-length Z and Y matrices.

To evaluate the influence of the passive structure on the propagation modes of the traveling-wave structure, EM simulations of a large number of different transmission line structures have been performed. This was done by sweeping the characteristic dimensions of the transmission line slice. Figure 5.17 shows these dimension parameters. Each parameter is swept across three or four values, resulting in a total of 432 possible combinations. Allowing the EM simulator a couple of days to complete and plugging in the MOS model, a parameterizable model of the traveling-wave MOS amplifier is obtained.

To avoid getting lost in the large amount of data generated by the parametric sweep, a tool

[1] These operations have been performed using the `NPort.recombine()` and `NPort.parallel()` methods of Python-nport (see Appendix C)

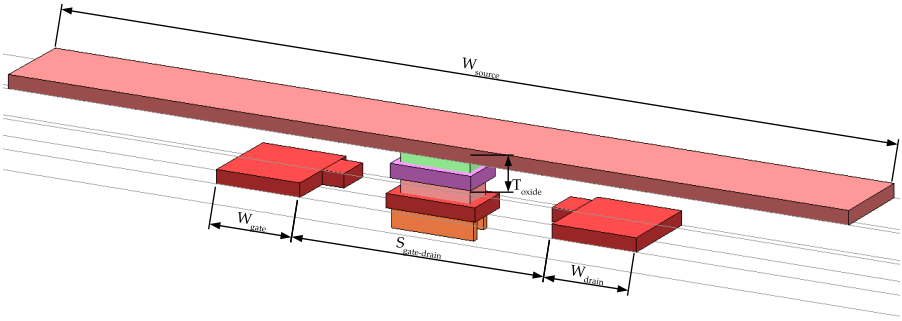


Figure 5.17: Sweeped geometric parameters in the unit slice of the growing-wave FET amplifier.

was developed to plot the propagation characteristics of each structure. A screenshot is shown in Figure 5.18. The application allows to visualize the impact of the transmission line's dimensions on the attenuation and phase constants and the eigenvectors. The tool also allows to scale each element of the approximating per-unit-length impedance and admittance matrices by some factor, allowing to easily visualize the individual effect of the different RLGC matrix elements.

Plugging in the model of a 5-µm wide NMOS transistor into the slice, we can explore the behavior of this combination for all 432 passive transmission line structures. Looking at the (approximate) per-unit-length conductance matrix elements in Figure 5.18, one can verify the effect of the MOSFET's transconductance. g_{12} (G12 in the figure) has a small negative value, indicating passive coupling, while g_{21} (G21) is large and positive, providing active coupling. The fact that g_{12} and g_{21} differ indicates that the conductive coupling is nonreciprocal. This is reflected in the eigenvector plots; there are no absolute even and odd modes as in a passively coupled transmission line. The mode where one eigenvector has a component in the opposite direction of the other eigenvector can be designated as the odd mode, however (the slow mode, in this case).

Changing g_{21} shows that the transconductance has little influence on the phase constant of the modes, but a large influence on the attenuation constant. Increasing g_{21} spreads the attenuation constants apart, making one mode more and the other less lossy, as shown in Figure 5.19. Also, altering $L_{12} = L_{21}$ and $C_{12} = C_{21}$, it is easy to confirm Farina's findings that inductive and capacitive coupling counteract. In the default structure, capacitive coupling is predominant and the fast mode is the most lossy mode. Decreasing capacitive coupling or increasing inductive coupling, the attenuation of the fast mode decreases, and that of the slow mode increases.

It is immediately apparent that it is not easy to obtain a growing mode. Only for two configurations of the passive transmission line slice, a growing mode is obtained. These two configurations are at the extremes of the sweep data, with very large dimensions, and even then the attenuation constant drops only barely below zero. Figure 5.20 shows the attenuation constants for the configuration showing the highest gain. Lowering the resistive losses helps to increase the gain, but this would require making the gate and

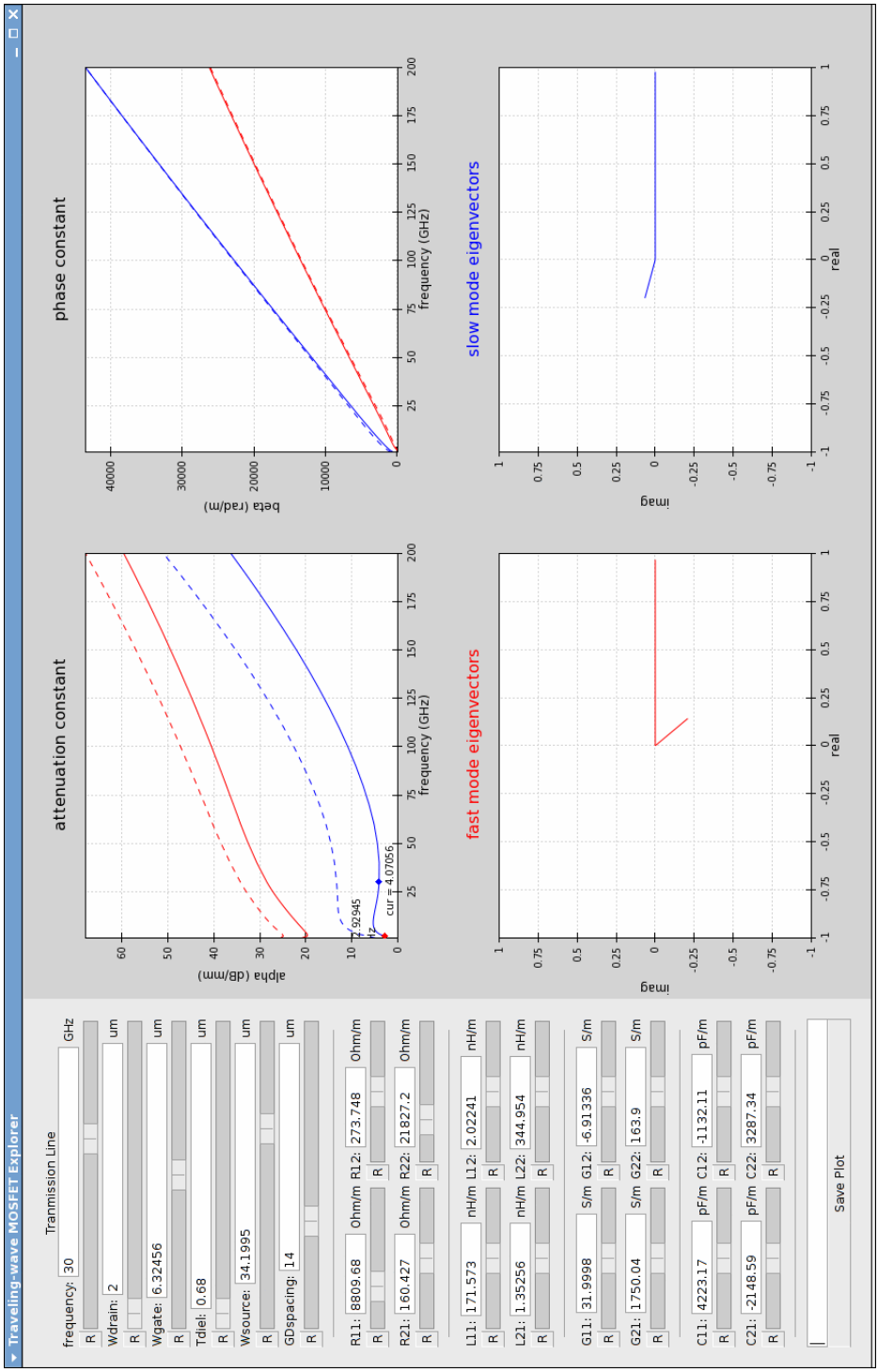


Figure 5.18: Traveling-wave MOSFET explorer screenshot. Sliders in the left-hand panel allow changing the geometry of the passive structure and the individual per-unit-length matrix elements. The two modes' attenuation (top left) and phase constants (top right) and the eigenvectors (bottom) are plotted.

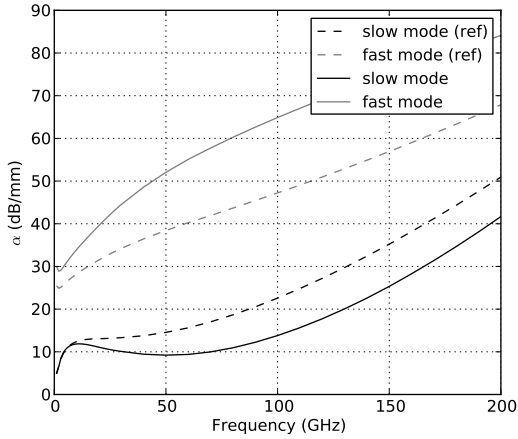


Figure 5.19: Slow and fast mode attenuation constants for the lumped growing-wave amplifier with $W_{\text{gate}} = 2$ µm, $W_{\text{drain}} = 6.33$ µm, $T_{\text{oxide}} = 2.68$ µm, $W_{\text{source}} = 34.2$ µm and $S_{\text{gate-drain}} = 14$ µm. The dashed lines show the attenuation constant for the realistic amplifier model, whereas the solid lines plot the attenuation constant for the model in which the g_{21} parameter has been doubled.

drain lines even wider.

5.3.2 Employing a Cross-Coupled Pair

Instead of relying on passive coupling, one can use a second transistor to actively couple the signal on the drain conductor back to the gate conductor. Of course, this is only realizable in a lumped growing-wave amplifier implementation. With the addition of the second MOSFET, a cross-coupled pair is formed, shown in Figure 5.21a, which is a well-known circuit for devising a negative resistance. The real part of the impedance seen between the drains of the FET pair is given by [Raz01]

$$\Re\{Z_{in}\} = -\frac{2}{g_m} \tag{5.21}$$

Unlike the single FET negative resistance circuit, the coupled pair does provide reciprocal coupling between gate and drain transmission line. Therefore, the negative resistance produced by the cross-coupled pair is closer to a "real" negative impedance, which is apparent from the conductance matrix derived from Figure 5.21b:

$$G = \begin{bmatrix} g_{ds} & g_m \\ g_m & g_{ds} \end{bmatrix} \tag{5.22}$$

Due to the reciprocal nature of the cross-coupled pair, passive coupling is no longer essential to obtain a growing wave. Also, because both the coupling from the gate to

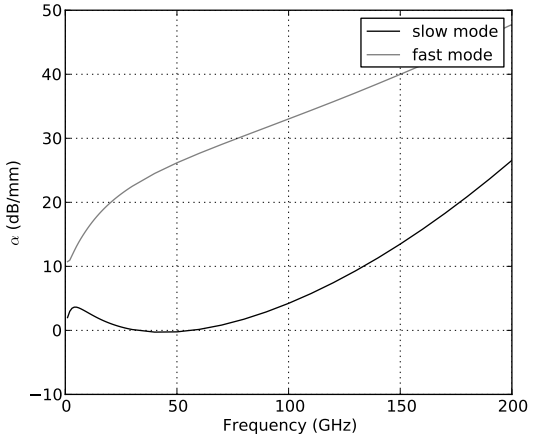
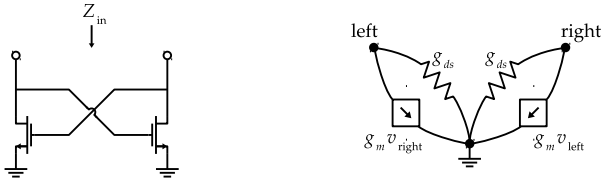


Figure 5.20: Slow and fast mode attenuation constants for $W_{\text{gate}} = W_{\text{drain}} = 20$ µm, $T_{\text{oxide}} = 2.68$ µm, $W_{\text{source}} = 100$ µm and $S_{\text{gate-drain}} = 30$ µm.



(a) (b)

Figure 5.21: Cross-coupled MOSFET pair: (a) schematic and (b) transmission line cross-section for determining the conductance matrix.

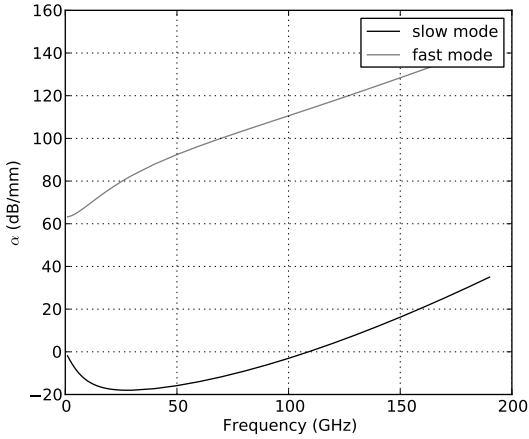


Figure 5.22: Slow and fast mode attenuation constants for the traveling-wave FET using cross-coupled cells with $W_{\text{gate}} = 2$ µm, $W_{\text{drain}} = 6.33$ µm, $T_{\text{oxide}} = 0.68$ µm, $W_{\text{source}} = 4$ µm and $S_{\text{gate-drain}} = 6$ µm.

the drain and vice versa are active, the growing mode is easier to obtain. Naturally, any passive coupling that is present still influences the operation of the traveling-wave FET.

To evaluate the use of the cross-coupled pair instead of a single transistor, two slices of the passive transmission line that was previously simulated are cascaded. In one slice, the MOSFET is connected as before, but in the other slice, the MOSFET's gate and drain are interchanged. With this configuration, a large gain is easily obtained, as is visible in Figure 5.22, with much smaller dimensions for the passive line features.

5.4 Stability of the Growing-Wave Amplifier

A uniform, continuous traveling-wave FET can, in theory, be stable. However, as soon as terminations are not perfect or when uniformity is disturbed, the device is very prone to instability. The reason for this is that the growing-wave FET is a longitudinally reciprocal device, meaning the propagation constants in the forward and backward directions are identical; the device amplifies signals in both directions. If the forward-traveling growing wave is reflected, a backward-traveling wave is produced and grows just like the forward-traveling wave. This backward-traveling wave can in turn be reflected, leading to oscillations.

5.4.1 Analyzing Stability

The growing-wave FET is fundamentally an active multiconductor transmission line. Stability in two-conductor active transmission lines has been studied by Rowe in 1964 in order to investigate the effect of imperfections in optical maser (laser) amplifiers [Row64a, Row64b]. Rowe investigates a simple uniform active transmission

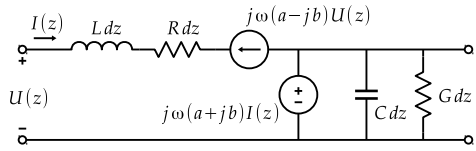


Figure 5.23: Equivalent circuit model for an an infinitesimal section of a non-reciprocal, non-symmetric transmission line.

line with discrete reflectors placed first at regular intervals and later at random intervals. The calculation is a tedious one but leads to an interesting conclusion. When no reflectors are present, the active transmission line is stable. However, even with reflectors, the line can still be stable. Unfortunately, this is only the case when reflections are very small, on the order of less than one percent. The fact that laser amplifiers have not found many uses has been attributed to this requirement [Kom72].

The grounded-source TWFET implementation discussed above is a 3-conductor transmission line where one of the two modes is active. The stability analysis as performed by Rowe but applied to a multiconductor would be even more involving due to the need for modal decomposition, but it seems safe to assume the analysis would lead to the same conclusion: the transmission line is only stable for reflection-less lines or for lines exhibiting very small reflections. As this would additionally require very good matching over the entire bandwidth where the attenuation constant is negative, it is highly unlikely a stable growing-wave FET can be produced.

5.4.2 Seeking Stability

While reflections are necessary to effectually cause oscillations, the longitudinally reciprocal nature of the growing-wave amplifier is a crucial factor in the development of oscillations. Therefore, breaking reciprocity is paramount in obtaining a stable growing-wave amplifier. Ideally, the line should have a negative attenuation constant in the forward direction and a large positive one in the backward direction.

5.4.2.1 Special Materials

Magnetic materials such as ferrites have a long history in microwave engineering, where they are used to realize non-reciprocal passive components such as circulators and isolators. Combined with an amplifying device, these materials can be used to build a growing-wave amplifier. For example, Hines distributes negative-resistance diodes along a microstrip transmission line [Hin70]. The microstrip line is placed on top of a magnetized ferrite slab, yielding different propagation properties in the forward and backward directions. Later, Paik presents a theoretical analysis of this amplifier configuration [Pai72]. However, stability of the amplifier is not studied in depth. It is only stated that the attenuation constant in the forward direction should be very small and that the backward attenuation constant is much larger.

Another possibility to obtain directionality is to employ metamaterials to introduce non-reciprocity into the transmission line. Just like the classic transmission line, a

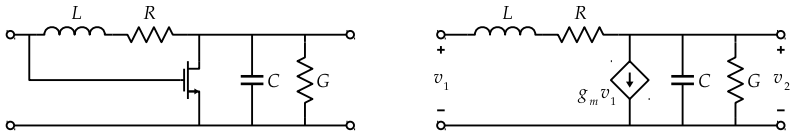


Figure 5.24: (a) Section of a lumped active transmission line with different properties in the forward and backward propagation direction and (b) its small-signal equivalent circuit.

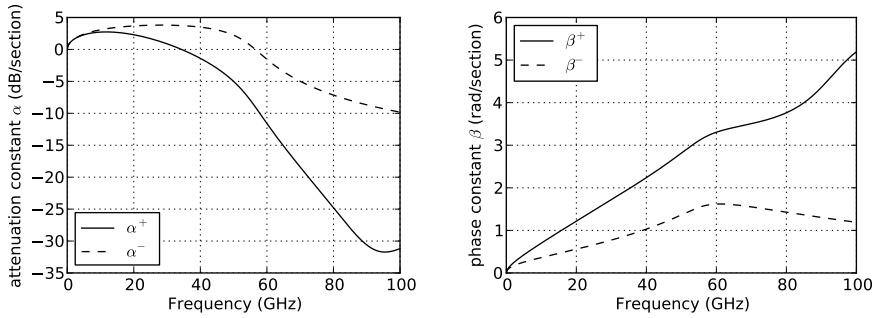
non-reciprocal and non-symmetric transmission line can be represented by an equivalent circuit model [Lin94]. This model, shown in Figure 5.23, includes, in addition to the *R*, *L*, *G* and *C* components, also a voltage-controlled current source and a current-controlled voltage source. The *a* and *b* parameters are due to respectively chirality (or non-symmetry) and non-reciprocity of the medium. Non-reciprocity of the material is responsible for non-symmetry of the transmission line and, vice versa, chirality of the material results in a non-reciprocal transmission line. More specifically, the propagation constants for the forward and backward directions are different provided the imaginary part of the chirality parameter *a* is non-zero [Fya97].

5.4.2.2 A Circuit Approach

As magnetic and metamaterials are not available in commercial CMOS processes, it makes sense to investigate the design of a lumped approximation to a non-reciprocal transmission line. The simple unit cell shown in Figure 5.24a exhibits different propagation properties for the forward and backward direction of propagation. Note that the small-signal circuit in Figure 5.24b shows a close resemblance to the non-reciprocal transmission line model of Figure 5.23. The MOSFET in Figure 5.24a provides a negative resistance in parallel with the inductor *L*, allowing for a growing wave. Non-reciprocity follows from the longitudinal asymmetry of the unit section.

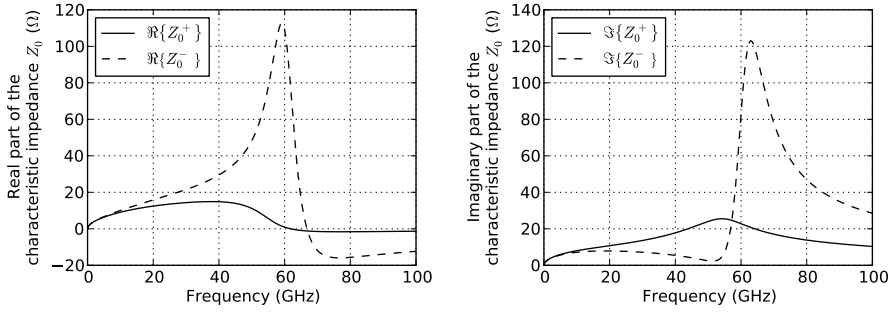
To investigate its properties, the forward and backward propagation constants and surge impedances of the unit section are determined using the equations derived in Appendix B, and are plotted in Figures 5.25 and 5.26 respectively; the propagations properties are indeed different for the two directions. For signals with a frequency between 35 and 55 GHz, forward-traveling waves are amplified ($\alpha^+ < 0$) and reverse-traveling waves are attenuated. However, backward attenuation in this frequency band α^- is still rather low, making the device prone to oscillation. Above 55 GHz, the line section amplifies in both directions and is guarantueed to be unstable.

The requirements for stable operation of the unit section can be qualitatively described with the help of the signal flow graph shown in Figure 5.27. The graph relates the voltages at the input and output nodes in terms of the propagation parameters. Roughly speaking, oscillation occurs when the loop gain from any node on this graph back to



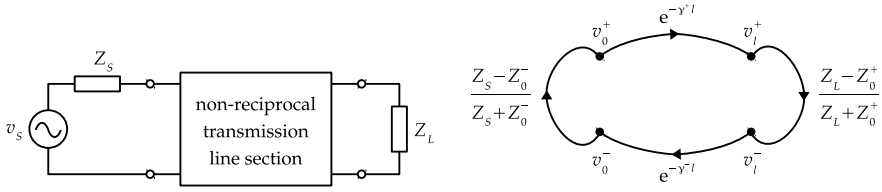
(a) (b)

Figure 5.25: Forward and backward propagation constants of the unit transmission line section of Figure 5.24a with $L = 120$ pH, $C = 120$ fF, $R = 0$ Ω and a 16×4 µm 130 nm NMOS transistor biased at 0.7 V (RF model):(a) attenuation constant and (b) phase constant. The $+$ and $-$ superscripts indicate forward- and backward-propagating waves, respectively.



(a) (b)

Figure 5.26: Characteristic impedance of the unit transmission line section of Figure 5.24a with $L = 120$ pH, $C = 120$ fF, $R = 0$ Ω and a 16×4 µm 130 nm NMOS transistor: (a) real part and (b) imaginary part.



(a) (b)

Figure 5.27: (a) Terminated non-reciprocal transmission line section and (b) signal flow graph representation of the voltages at the input and output.

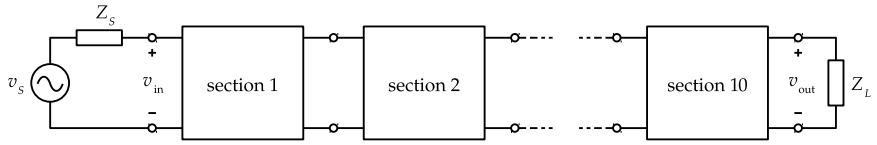


Figure 5.28: Simulation setup for a 10-section growing-wave amplifier. The source and load impedance are chosen to match the backward and forward characteristic impedances of the lumped transmission line.

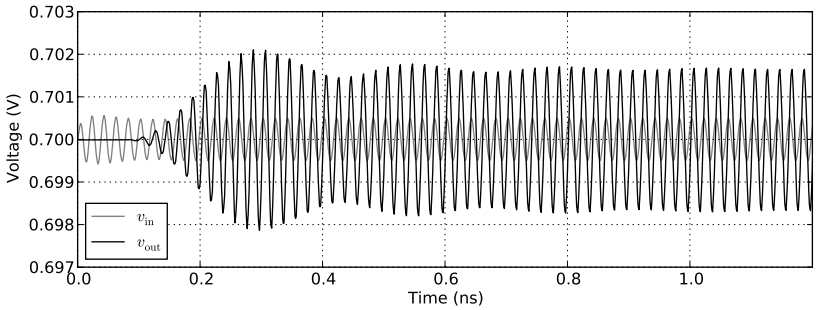


Figure 5.29: Transient simulation waveforms of a 10-section growing-wave amplifier.

itself,

$$\left| \frac{Z_L - Z_0^+}{Z_L + Z_0^+} \cdot \frac{Z_S - Z_0^-}{Z_S + Z_0^-} \cdot e^{-(\gamma^+ + \gamma^-)l} \right|, \tag{5.23}$$

exceeds 1. Conversely, stability is maximized when (5.23) is minimized. To this effect, the source and load impedances, Z_S and Z_L should approximate, respectively, the backward and forward characteristic impedances, Z_0^- and Z_0^+, as closely as possible. Additionally, the sum of the forward and backward attenuation constants should be as large as possible. While the latter requirement is not quite complied with for our example transmission line section, simulations do show that a chain of these sections can amplify a signal, and at the least maintain marginal stability. Choosing source and load impedances to match the characteristic impedances at 50 GHz, a 10-section growing-wave amplifier (Figure 5.28) can amplify a 50 GHz sine wave, as shown in Figure 5.29. The initial ringing of the output waveform indicates that the amplifier is prone to oscillation.

In order to increase the amplifier's gain, the number of sections can simply be increased. However, when the signal amplitude exceeds a critical value, non-linearity of the transistor affects the propagation parameters of the transmission line; matching is degraded and the circuit starts to oscillate.

5.5 Conclusion

The traveling-wave transistor has a long history. Originally conceived as a continuous version of the classic distributed amplifier, it was later discovered that the device can additionally support another mode of operation, capable of propagating an exponentially-growing wave. While the former mode of operation can help to further extend the bandwidth of the distributed amplifier, the latter can possibly overcome the gain limitation of the classic distributed amplifier. For this reason, the focus of this chapter is the growing-wave amplifier.

This mode of operation is vaguely attributed to the presence of a negative resistance, produced by the transconductance. In an attempt to clarify the principle of operation of the growing-wave amplifier, the traveling-wave amplifier is modeled as an active transmission line; that is, with a negative attenuation constant. First, a basic two-conductor active transmission line model is presented that is used to link the concept of negative impedance to the growing mode. The insights obtained from that analysis are then transferred to a three-conductor transmission line model. Based on this model, the requirements for obtaining a growing mode are discussed.

The model is then applied to the design of a lumped growing-wave amplifier in CMOS. An exploration of the design space teaches us that it is not easy to build an amplifier capable of bringing forth a growing mode. The few configurations featuring a negative attenuation constant show only a very low gain. It is, however, discovered that providing active coupling between the two signal conductors in both directions makes it much easier to obtain the growing mode. This is achieved by making use of a cross-coupled NMOS pair in each unit amplifier section, as opposed to only a single transistor. With this configuration, it is easy to obtain a large negative attenuation constant across a large bandwidth.

Unfortunately, whether making use of a cross-coupled pair or not, the traveling-wave FET is prone to become unstable. While some of the publications discussed in the beginning of this chapter did warn about instabilities, the stability of the traveling-wave FET was never thoroughly investigated. While it is theoretically possible to operate a growing-wave in a stable way, this requires near-perfect input and output termination across the frequency band where the attenuation constant is negative. The latter is impossible to achieve in a realistic setting.

The longitudinal reciprocity of the growing-wave amplifier is a crucial factor in the development of oscillations. While the traveling-wave FET presented in literature does exhibit non-reciprocal coupling between the conductors of the transmission line, it is still longitudinally reciprocal, featuring identical propagation constants in the forward and backward directions. Since signals are amplified equally in both directions, any reflection leads to oscillations. To improve the stability, the device should be non-reciprocal, and more specifically, the attenuation constant in the backward direction should be positive. To this end, a passive non-reciprocal transmission line can be periodically loaded with negative-resistance components to build a stable growing-wave amplifier. Non-reciprocal transmission lines can be realized using magnetic or metamaterials.

Since these materials are not available in commercial CMOS processes, the design of a lumped non-reciprocal growing-wave amplifier was investigated. Using a fairly simple unit cell employing an inductor, a capacitor and a single NMOS transistor, simulations show it is possible to build a stable growing-wave amplifier. The gain of this amplifier can be increased by simply cascading more unit cells.

Chapter 6

Conclusion

6.1 General Conclusions

This work presents the results of the author's research on distributed amplification and can be subdivided in two parts. In a first part, the feasibility of using distributed amplifiers for low-power applications has been studied. The work includes investigation of novel distributed amplifier topologies such as the distributed amplifier with improved output line tapering and the tapered matrix amplifier. The merits of the concepts and ideas presented have been validated with a prototype low-power broadband amplifier. A second part of the work treats the traveling-wave transistor. Originally conceived as a continuous version of the distributed amplifier, the structure can also support a growing wave, which theoretically allows the gain to grow indefinitely with transistor width.

Chapter 1 looks at some applications of broadband amplifiers. Recent trends in data communication call for amplifiers capable of amplifying signals across a broad band of frequencies. As the distributed amplifier is not the only broadband amplifier topology out there, the basic operation of broadband amplifier topologies, including the distributed amplifier, are briefly reviewed and their advantages and disadvantages are discussed. Also, a short overview of the different types of IC technologies is given, in which the significance of CMOS is highlighted.

An introduction to distributed amplification is found in Chapter 2. First, the basic operating principle of the distributed amplifier is reviewed. The implementation of the transmission lines in a distributed amplifier using LC ladders or periodically-loaded lines and how they determine the frequency response of the amplifier are examined. The effects of losses in the transmission lines and gain cell parasitics are also covered, followed by the discussion of noise and distortion in the classic distributed amplifier. The remainder of the chapter covers the variations to the distributed amplifier that have been presented in literature; these include the cascaded-single-stage, matrix and tapered distributed amplifiers and the mystifying distributed amplifier with internal feedback.

Chapter 3 looks at the distributed amplifier through low-power goggles. Tapering of the output transmission line goes a long way in boosting the gain-to-power consumption ratio of the distributed amplifier. The conventional tapering scheme does require a lowered load impedance though, limiting its use. To improve on this, a general expression governing the correct operation of the distributed amplifier with tapered output line is derived, enabling the determination of an improved tapering scheme. The new tapering scheme suffers from two conflicting requirements regarding the leftmost

gain cell, but the effect of this conflict can be minimized. Additionally, the noise performance of the tapered distributed amplifier is qualitatively shown to be similar to that of a classic distributed amplifier with the same gain and bandwidth. The new tapered matrix amplifier topology, a combination of the matrix amplifier concept and transmission line tapering, is introduced, allowing to further improve the efficiency. In addition to these, a number of techniques to improve the efficiency of distributed amplifiers in general are discussed.

The design of a low-power 15 dB, 20 GHz amplifier in a 90 nm CMOS technology is covered in Chapter 4. Using the techniques of Chapter 3, a 2×2 tapered matrix amplifier is optimized for lowest power consumption given the gain and bandwidth requirements. Because of the large number of parasitic and other effects complicating the design, a pragmatic approach employing circuit optimization is presented. To accommodate the optimizer, the topology is first mutated in order to enable larger transistors to be used. Practical aspects of the optimization and layout of the circuit are discussed in detail. The overall performance of the prototype is found to be very competitive with low-power broadband amplifiers found in literature. The power consumption of only 12.9 mW presents a record for the given gain and bandwidth. The Achilles heel of the prototype is its linearity; the IIP3 is among the lowest of the amplifiers in the comparison. Therefore, the chapter is concluded with a section revisiting the design of the amplifier, with as target improving the linearity performance, but keeping the power consumption to a minimum. Adjustments in biasing and resistive degeneration of the second-stage transistors allow to improve the IIP3 by 10 dB, at the cost of increasing the power consumption by only 70 %.

Chapter 5 examines the traveling-wave transistor. First, the long history of research on the device is summarized. In this discussion, it becomes clear that the traveling-wave transistor is capable of operating in two different modes. One of these corresponds to the operation of the classic distributed amplifier, while the other allows for an exponentially growing wave. The latter makes it possible to obtain any amount of gain by simply making the device wider (not considering compression or breakdown). However, it is not clear how exactly to build the device so that it can support the growing mode. Starting from a simple two-conductor transmission line model, the basic mechanisms of the exponential mode are investigated. This is then extended to a full three-conductor model, capable of accurately modeling a traveling-wave FET with the source and bulk shorted. Using eigenanalysis, the growing mode can be analyzed. The latter model is then applied to the design of a growing-wave amplifier in CMOS. It is shown that the design of such an amplifier is all hampered by intrinsic losses and the maximum dimensions of the transmission line in a monolithic process. However, based on the insights acquired, an alternative traveling-wave amplifier topology using cross-coupled pairs is proposed, making it much easier to obtain a growing wave. However, due to the fact that the traveling-wave transistor is a longitudinally reciprocal device – that is, it amplifies signals in the reverse as well as in the forward directions – it is extremely prone to instability. Finally, the use of non-reciprocal transmission lines are suggested for the design of a stable growing-wave amplifier. As the materials required to realize non-reciprocal properties are not available in commercial CMOS processes, an attempt is made to design a lumped non-reciprocal growing-wave amplifier. Simulations

demonstrate that careful input and output termination allows for stable operation while amplifying a 50 GHz signal.

6.2 Main Contributions

These are believed to be the original contributions to the state of the art of distributed amplification:

- A general expression that governs the proper operation of the tapered distributed amplifier was derived. It allows deriving the transmission line sections' required characteristic impedances as a function of the relative sizes of the gain cells. This allows the conception of new catering schemes to cater for different requirements.

- Based on this expression, a new tapering scheme was presented that allows for a larger load impedance, improving power gain and eliminating the need for a very bulky and lossy impedance transformation network.

- A qualitative noise analysis of the tapered distributed amplifier has been performed. While it at first seems that the noise performance of the tapered amplifier is much worse compared to its classic counterpart, it was found that the presence of losses paradoxically improves matters a lot.

- A new amplifier topology, the tapered matrix amplifier, was introduced. Inspired by the matrix amplifier, but not sharing that topology's inherent non-flat gain property, the tapered matrix amplifier enjoys the multiplication of the gain of its stages, improving the gain-to-power consumption ratio.

- A prototype tapered matrix amplifier was realized in a 90 nm CMOS technology. The amplifier features a record gain-bandwidth-to-power consumption ratio, proving that distributed amplification is indeed suitable for low-power applications. Additionally, the noise figure and die area are competitive with other realized amplifier topologies.

- The prototype design was revisited to boost the linearity of the amplifier. The new design shows that high linearity and a low power consumption can be reconciled in a tapered matrix amplifier design.

- The operating principles behind the exponentially-growing mode of the traveling-wave transistor have been analyzed and illustrated. Based on this knowledge, a new circuit topology employing cross-coupled FETs was presented that more readily supports the growing mode.

- Concerns about the stability of the growing-wave amplifier are investigated and confirmed. It is shown that stability can be improved by introducing non-reciprocity. The latter is illustrated by simulations of a non-reciprocal lumped unit cell which, when cascaded, can amplify a signal while maintaining stability.

- A number of software tools were developed in support of the work presented in this text (see Appendix C). Python-substratestack helps to manage the substrate stack data required by EM field solvers. Python-nport provides high-level abstraction for n-port data and includes support for non-reciprocal multiconductor transmission lines. The latter was heavily used in the work on the traveling-wave transistor.

6.3 Suggestions for Future Work

While the tapered matrix amplifier prototype does have a very good overall performance and clearly shows the merits of the techniques presented in this text, the design heavily relies on optimization. This was necessary due to the number of non-idealities and their considerable influence on the amplifier's operation. Of these, the parasitic feedback-capacitance C_{gd} of the common-source gain cells has the most profound impact on the operation of the amplifier. The use of cascode gain cells can largely eliminate the effect of this capacitance. However, it also roughly doubles the amplifier's power consumption, and the use of cascode gain cells was avoided for this reason. However, from Figure 2.19a, one can see that the presence of C_{gd} nearly halves the bandwidth of the amplifier. The GBW-to-power consumption ratio of the cascode-based variant will therefore be very close to that of the common-source-based amplifier. For this reason, it is worthwhile to investigate the design of a tapered matrix amplifier using cascode gain cells. The increased reverse isolation offered by cascode cells is expected to make the design of the amplifier more straightforward, as it will more closely match the theoretical model and the reliance on optimization can be reduced.

The presented low-power distributed amplifier lends itself for use as a low-noise amplifier. Although the noise performance was not optimized, the noise figure holds up well against amplifiers with similar specifications. The design of a tapered matrix amplifier that specifically focuses on noise performance should be able to further reduce the noise figure, and is therefore worth looking into.

It is interesting to look into the design of a differential version of the tapered matrix amplifier. A differential version of the classic distributed amplifier was already shown to have some advantages compared to the single-ended version [Ahn02]. For instance, a differential implementation offers improved immunity against common-mode substrate noise and suppresses even harmonics, improving linearity. The price to pay is roughly a doubling of the power consumption and required die area. An added extra is the opportunity to use cross-coupled capacitors to neutralize the Miller capacitance of the FETs [Lee04a], mitigating the negative effects of the latter.

The use of a non-reciprocal unit cell as the basis of a growing-wave amplifier looks promising. The stability of the presented unit cell, however, could be improved upon. Also, the parasitics of the inductor were not taken into account, as well as details pertaining to biasing of the transistor in the unit cell. A thorough investigation of these is necessary before a stable growing-wave amplifier can be produced. In addition, alternative unit cell topologies with increased reverse isolation should be explored, in order to improve the stability of the amplifier. Alternatively, the use of magnetic or metamaterials should be investigated. These could enable the realization of stable

growing-wave amplifiers operating at very high frequencies.

Appendix A

Understanding Scattering Parameters

Scattering parameters, or S-parameters for short, are used to model the steady-state behavior of linear electrical networks [And96]. Both passive and active networks can be represented by S-parameters. If the response of the network is non-linear, the parameters can only represent the small-signal behavior for any particular bias point. Similar to impedance (Z) and admittance (Y) parameters, an N-port network is modeled by a square matrix with a dimension equal to the number of ports[1]. Where Z- and Y-parameters express the relation between voltages across and currents flowing into the ports of the network, S-parameters relate the so-called *traveling waves* that flow into the ports to the reflected waves. For a two-port network, the scattering matrix equation is given by

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}, \tag{A.1}$$

in which a_1 and a_2 represent the incident voltage waves at port 1 and port 2 respectively, and b_1 and b_2 represent the reflected voltages waves. These voltage waves are also depicted in Figure A.1. To capture frequency-dependent effects, a network is typically modeled by a set of scattering matrices, one for each frequency sample.

Scattering parameters are defined with respect to a reference impedance Z_0. This impedance is equal to the source and load impedance used for measuring the S-parameters.

While S-parameters are able to model the behavior of transistors, custom transistor models such as BSIM offer a much more comprehensive model that includes bias-dependence, non-linearities and noise. In RFIC design, S-parameters are therefore typically only used to model passive networks such as inductors, transformers and transmission lines. EM simulators such as Agilent Momentum and Sonnet em can

[1] A port is a pair of terminals in which the current flowing into one terminal is the same as the current flowing out of the other [Gra01].

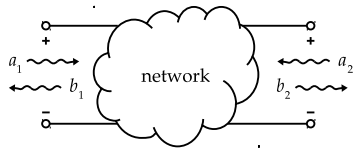


Figure A.1: Incident and reflected traveling waves at the ports of a two-port network.

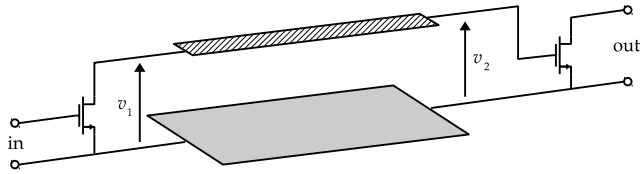


Figure A.2: A simple amplifier circuit consisting of a microstrip line connecting two FETs.

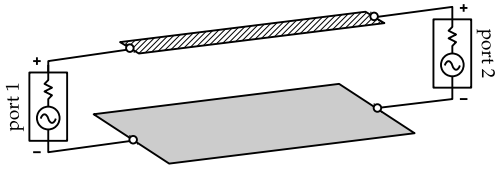


Figure A.3: Placement of ports on the microstrip line for simulation in an EM solver.

export their simulation results as S-parameters, which are then combined with transistor models by a circuit simulator to model the RF circuit. The use of the S-parameters in a circuit simulator is not as straightforward as it seems at first sight, and is therefore a common source of confusion.

A.1 S-Parameters in Field Solvers

Imagine we need to simulate the simple circuit including a microstrip line depicted in Figure A.2. Simulating the microstrip in an EM simulator requires placing ports on the layout, as shown in Figure A.3. In planar EM solvers such as Agilent Momentum and Sonnet em, a port can be placed by indicating only a single point on the layout, even though a port consists of two terminals. This is because the reference terminal is implicit in this case, chosen at the same coordinates on an ideal ground conductor at the bottom of the substrate stack. This implicit choice of reference terminals stems from the fact that the primary use of planar EM solvers was for RF PCB design, in which a low-resistive ground plane typically covers the full PCB. Unfortunately, this leads to some confusion in RFIC design, where there is no ground plane at the bottom of the stack. Therefore, it is recommended to explicitly define a reference terminal for each port so that the actual current return path is modeled correctly.

For the microstrip of Figure A.3 the scattering parameters output by the EM solver basically relate the voltages across ports 1 and 2. It is important to note that the parameters do not include any information about the voltage between terminals of two different ports. For example, the voltage between the reference terminals of port 1 and 2 is not defined[2]. However, this information is, in general, not necessary to correctly model the circuit, as the effect of the ground plane (phase shift, attenuation) is included in the S-parameter data. Figure A.4 shows a lumped-element representation of the

[2]In fact, the voltage between any two points that lie far apart, electrically speaking, is not always uniquely defined [Col01]. For this reason, it is important to place the terminals of a port close together [Boh08]

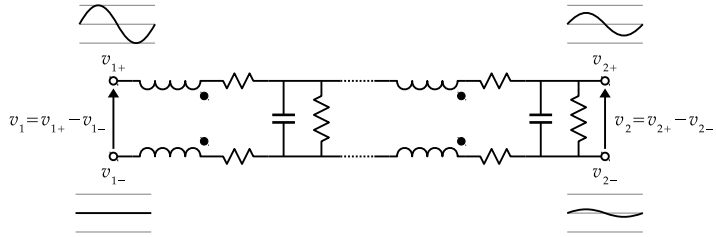


Figure A.4: Lumped model of the microstrip line. The potentials at the four terminals are indicated.

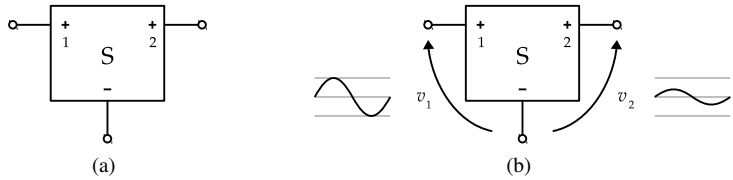


Figure A.5: Representation of a two-port S-parameter model with a three-terminal black box: (a) symbol, and (b) port voltages

microstrip line of Figure A.2. The waveforms in the figure indicate the potential at the four terminals when a sinusoidal signal is applied at port 1. Due to capacitive and inductive coupling, the signal is coupled to the ground conductor and a weak copy appears at the reference terminal of port 2. Similarly, the signal on the + terminal of port 2 is weakened due to resistive losses. Although information about the potentials on the individual nodes is lost, the effect of the ground plane of the microstrip line is included in the relation between the port voltages v_1 and v_2.

A.2 S-parameters in Circuit Simulators

S-parameter data can be represented in two ways in circuit simulators. In EEsof ADS, n-port S-parameter data is represented by a black box with $n+1$ terminals. Figure A.5a shows the representation of our two-port microstrip line, for example. In this representation, all ports share a single reference node. This is another source of confusion with S-parameters, as some may be tempted to think that the reference nodes in the modeled network are short-circuited and information has been lost. However, the reference node is just that, a reference. Referring back to Figure A.4, the S-parameter box of Figure A.5b relates the port voltages v_1 and v_2 to each other and thus includes the effect of the ground plane [Cor03].

Figure A.6 shows a circuit model of the network of Figure A.2. Because the S-parameter box has only a single reference node, the sources of the two FETs are connected together in the circuit model. Some may incorrectly think that this implies that they are at the same potential in the actual circuit. Confusion originates from the fact that there is not a one-to-one relationship between nodes in the circuit model and physical terminals in the

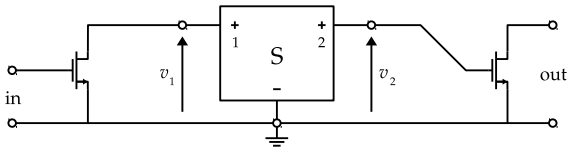
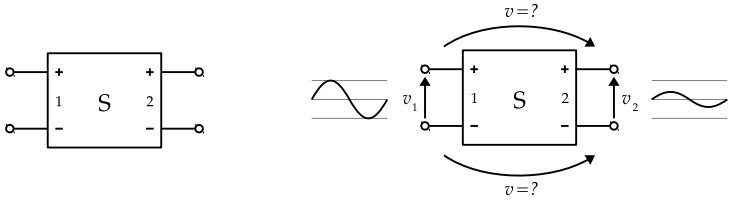


Figure A.6: Circuit schematic of the circuit of Figure A.2 in which the microstrip line is modeled using S-parameters.



(a) (b)

Figure A.7: Representation of a two-port S-parameter model with a four-terminal black box: (a) symbol, and (b) port voltages

actual circuit. However, to model the effect of the microstrip line, it is only important to model the relation between the voltages v_1 and v_2, and this requirement is satisfied; the circuit model shown in Figure A.6 is complete and faithful.

In contrast to ADS, Cadence Virtuoso represents an n-port S-parameter model by a $2n$-terminal box, as shown in Figure A.7a for the microstrip line. Even though each port now has a separate reference terminal, the S-parameters still contain the same information as before. The voltage between any two reference terminals is undefined, as illustrated in Figure A.7b. It is left to the user to set the voltage between the reference nodes. Simply short-circuiting them, one obtains the $n+1$ terminal representation of Figure A.5a.

As the voltage across each port is defined, the voltage between the positive terminals of two ports can also be calculated, as shown in Figure A.8. However, this does not correspond to a physical voltage since it also includes the relation between the reference nodes of the ports.

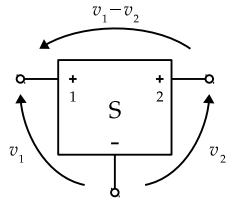


Figure A.8: The voltage between the positive terminals of two ports.

Appendix B

Generalized Modal Analysis of Non-reciprocal Non-uniform Multiconductor Transmission Lines

Faria presented a generalized modal analysis theory for non-uniform multiconductor transmission lines [Far04]. The analysis is simplified by the assumption of reciprocal lines, but limiting its application to passive transmission lines. In this appendix, the analysis is extended to the general case, allowing it to be applied to the growing-wave amplifier. For details and background information on the analysis, we refer to the original publication by Faria. The analysis presented here uses the same notation.

B.1 Extension to Nonreciprocal Transmission Lines

Coordinate transformations between the phase and modal voltages and currents are defined by Faria using the $\mathbf{T}_0$, $\mathbf{T}_\ell$ and $\mathbf{W}_0$, $\mathbf{W}_\ell$ matrices, respectively:

$$\hat{\mathbf{A}} = \mathbf{T}_0^{-1}\mathbf{A}\mathbf{T}_\ell \tag{B.1a}$$

$$\hat{\mathbf{B}} = \mathbf{T}_0^{-1}\mathbf{B}\mathbf{W}_\ell \tag{B.1b}$$

$$\hat{\mathbf{C}} = \mathbf{W}_0^{-1}\mathbf{C}\mathbf{T}_\ell \tag{B.1c}$$

$$\hat{\mathbf{D}} = \mathbf{W}_0^{-1}\mathbf{D}\mathbf{W}_\ell, \tag{B.1d}$$

where $\hat{\mathbf{A}}$, $\hat{\mathbf{B}}$, $\hat{\mathbf{C}}$ and $\hat{\mathbf{D}}$ are the diagonal modal domain transmission matrices. The indices 0 and ℓ correspond, respectively, to the sending and receiving ends of the multi-conductor transmission line.

Under the assumption of reciprocity, Faria shows that $\mathbf{W}_0$ and $\mathbf{W}_\ell$ can be calculated from $\mathbf{T}_0$ and $\mathbf{T}_\ell$, reducing the number of required computations. For non-reciprocal transmission lines, this is not the case, and the coordinate transformation matrices need to be calculated in a different way. Eliminating $\mathbf{T}_0$ and $\mathbf{W}_0$ from (B.1), yields

$$\mathbf{A}\mathbf{T}_\ell\hat{\mathbf{A}}^{-1} = \mathbf{B}\mathbf{W}_\ell\hat{\mathbf{B}}^{-1} \tag{B.2a}$$

$$\mathbf{C}\mathbf{T}_\ell\hat{\mathbf{C}}^{-1} = \mathbf{D}\mathbf{W}_\ell\hat{\mathbf{D}}^{-1}. \tag{B.2b}$$

Rearranging the above, we find

$$\mathbf{T}_\ell^{-1}\mathbf{A}^{-1}\mathbf{B}\mathbf{W}_\ell = \hat{\mathbf{A}}^{-1}\hat{\mathbf{B}} \tag{B.3a}$$

$$\mathbf{W}_\ell^{-1}\mathbf{D}^{-1}\mathbf{C}\mathbf{T}_\ell = \hat{\mathbf{D}}^{-1}\hat{\mathbf{C}}. \tag{B.3b}$$

Finally, left- and right-multiplying these, yields

$$\mathbf{T}_\ell^{-1}\mathbf{A}^{-1}\mathbf{B}\mathbf{D}^{-1}\mathbf{C}\mathbf{T}_\ell = \hat{\mathbf{A}}^{-1}\hat{\mathbf{B}}\hat{\mathbf{D}}^{-1}\hat{\mathbf{C}} \tag{B.4a}$$

$$\mathbf{W}_\ell^{-1}\mathbf{D}^{-1}\mathbf{C}\mathbf{A}^{-1}\mathbf{B}\mathbf{W}_\ell = \hat{\mathbf{D}}^{-1}\hat{\mathbf{C}}\hat{\mathbf{A}}^{-1}\hat{\mathbf{B}}. \tag{B.4b}$$

This result defines $\mathbf{T}_\ell$ and $\mathbf{W}_\ell$ as the similarity transformation matrices that respectively bring the matrices $\mathbf{A}^{-1}\mathbf{B}\mathbf{D}^{-1}\mathbf{C}$ and $\mathbf{D}^{-1}\mathbf{C}\mathbf{A}^{-1}\mathbf{B}$ into diagonal form.

Analogous to the preceding derivation, eliminating $\mathbf{T}_\ell^{-1}$ and $\mathbf{W}_\ell^{-1}$ from (B.1) and rearranging, we get

$$\mathbf{T}_0^{-1}\mathbf{A}\mathbf{C}^{-1}\mathbf{W}_0 = \hat{\mathbf{A}}\hat{\mathbf{C}}^{-1} \tag{B.5a}$$

$$\mathbf{W}_0^{-1}\mathbf{D}\mathbf{B}^{-1}\mathbf{T}_0 = \hat{\mathbf{D}}\hat{\mathbf{B}}^{-1}. \tag{B.5b}$$

Again, left- and right-multiplication allows for the calculation of $\mathbf{T}_0$ and $\mathbf{W}_0$:

$$\mathbf{T}_0^{-1}\mathbf{A}\mathbf{C}^{-1}\mathbf{D}\mathbf{B}^{-1}\mathbf{T}_0 = \hat{\mathbf{A}}\hat{\mathbf{C}}^{-1}\hat{\mathbf{D}}\hat{\mathbf{B}}^{-1} \tag{B.6a}$$

$$\mathbf{W}_0^{-1}\mathbf{D}\mathbf{B}^{-1}\mathbf{A}\mathbf{C}^{-1}\mathbf{W}_0 = \hat{\mathbf{D}}\hat{\mathbf{B}}^{-1}\hat{\mathbf{A}}\hat{\mathbf{C}}^{-1}. \tag{B.6b}$$

With $\mathbf{T}_0$, $\mathbf{T}_\ell$, $\mathbf{W}_0$ and $\mathbf{W}_\ell$ known, the diagonal modal matrices $\hat{\mathbf{A}}$, $\hat{\mathbf{B}}$, $\hat{\mathbf{C}}$ and $\hat{\mathbf{D}}$ can be calculated, and from these, the propagation constants and surge (characteristic) impedances of each mode. The expressions derived by Faria for the latter two also assume reciprocity. In general, the propagation constants for the forward and backward directions are not equal. For forward-traveling waves, we get

$$e^{-\hat{g}_k^{(f)}\ell} = \frac{2}{\left(\hat{a}_k+\hat{d}_k\right)+\sqrt{\left(\hat{a}_k+\hat{d}_k\right)^2-4\left(\hat{a}_k\hat{d}_k-\hat{b}_k\hat{c}_k\right)}}, \tag{B.7}$$

and

$$\hat{z}_k^{(f)} = \frac{\sqrt{\left(\hat{a}_k+\hat{d}_k\right)^2-4\left(\hat{a}_k\hat{d}_k-\hat{b}_k\hat{c}_k\right)}+\left(\hat{a}_k-\hat{d}_k\right)}{2\hat{c}_k}. \tag{B.8}$$

For backward-traveling waves, these evaluate to

$$e^{-\hat{g}_k^{(b)}\ell} = \frac{\left(\hat{a}_k+\hat{d}_k\right)-\sqrt{\left(\hat{a}_k+\hat{d}_k\right)^2-4\left(\hat{a}_k\hat{d}_k-\hat{b}_k\hat{c}_k\right)}}{2}, \tag{B.9}$$

and

$$\hat{z}_k^{(b)} = \frac{\sqrt{\left(\hat{a}_k+\hat{d}_k\right)^2-4\left(\hat{a}_k\hat{d}_k-\hat{b}_k\hat{c}_k\right)}-\left(\hat{a}_k-\hat{d}_k\right)}{2\hat{c}_k}. \tag{B.10}$$

For reciprocal transmission lines,

$$\hat{a}_k\hat{d}_k-\hat{b}_k\hat{c}_k = 1 \tag{B.11}$$

and the forward and backward propagation constants, (B.7) and (B.9), can be readily shown to be equal. Similarly, the surge impedances in the forward and backward

directions, (B.8) and (B.10), are equal when the transmission line is symmetric, for which

$$\hat{a}_k = \hat{d}_k. \tag{B.12}$$

The transmission matrix elements can also be written as a function of the propagation constants and surge impedances:

$$\hat{a}_k = \frac{\hat{z}_k^{(f)} e^{\hat{g}_k^{(f)}\ell} + \hat{z}_k^{(b)} e^{-\hat{g}_k^{(b)}\ell}}{\hat{z}_k^{(f)} + \hat{z}_k^{(b)}} \tag{B.13a}$$

$$\hat{b}_k = \frac{\left(e^{\hat{g}_k^{(f)}\ell} - e^{-\hat{g}_k^{(b)}\ell}\right) \hat{z}_k^{(f)} \hat{z}_k^{(b)}}{\hat{z}_k^{(f)} + \hat{z}_k^{(b)}} \tag{B.13b}$$

$$\hat{c}_k = \frac{e^{\hat{g}_k^{(f)}\ell} - e^{-\hat{g}_k^{(b)}\ell}}{\hat{z}_k^{(f)} + \hat{z}_k^{(b)}} \tag{B.13c}$$

$$\hat{d}_k = \frac{\hat{z}_k^{(b)} e^{\hat{g}_k^{(f)}\ell} + \hat{z}_k^{(f)} e^{-\hat{g}_k^{(b)}\ell}}{\hat{z}_k^{(f)} + \hat{z}_k^{(b)}} \tag{B.13d}$$

Note that

$$\hat{a}_k \hat{d}_k - \hat{b}_k \hat{c}_k = e^{\hat{g}_k^{(f)}\ell} e^{-\hat{g}_k^{(b)}}, \tag{B.14}$$

which equals 1 when the forward and backward propagation constants are equal.

Finally, it is worth noting that the expressions relating the modal transmission matrix elements to the modal propagation constants and surge impedances are also valid for two-conductor transmission lines, in which case the scalar transmission parameters may be directly used in the expressions without the need for modal decomposition.

B.2 Notes on Numerical Computation

With the application of the results obtained above (or those for reciprocal lines by Faria), a number of problems surface. These are briefly discussed in this section and the reader is also pointed to solutions.

B.2.1 Numerical Stability

Just like with the diagonalization of the **ZY** matrix for uniform transmission lines, the diagonalization of the transmission matrices can suffer from eigenvalues that are close neighbors. The latter can result in inaccuracies in the numerical computation of the eigenvalues. To spread out the eigenvalues, and consequently make the computation well conditioned, it suffices to subtract from the matrix its trace divided by the number of rows/columns in the matrix [Far93]. The eigenvalues of the resulting matrix simply need to be shifted back afterward.

B.2.2 Eigenvalue Sorting

For practical transmission lines, the concept of frequency enters the picture. Physically realizable transmission lines typically show a frequency dependency, and therefore need to be modeled with an array of ABCD matrices, one for each frequency sample. As long as the frequency samples are close enough together, the modal propagation constants and surge impedances vary smoothly.

However, the eigenvalues and eigenvectors are calculated separately for each frequency point, and their ordering is not defined. To make things worse, the sign of the eigenvectors is arbitrary, and the eigenvalues of two modes can cross over. These effects make it difficult to consistently assign the eigenvalues and -vectors for all frequency points to the different modes. For this reason, the eigenvalues need to be sorted. An example of an algorithm performing eigenvalue sorting is contained in the Eigenshuffle MATLAB function by John D'Errico [D'E].

B.2.3 Phase Unwrapping

Even if the eigenvalues are consistently sorted, the propagation constant and surge impedance can still show large jumps from one frequency sample to another. This stems from the use of the principal value returned by the complex square-root and logarithm functions. As both these functions are defined in terms of the polar form of the complex argument

$$z = re^{j\theta}, \tag{B.15}$$

the phase θ can be unwrapped to obtain consistent results for the propagation constant and surge impedance. The "unwrapped" complex square root is defined as

$$\sqrt{z} = \sqrt{r}e^{i\frac{\theta}{2}}, \tag{B.16}$$

and the natural logarithm as

$$\log z = \log r + i\theta. \tag{B.17}$$

Appendix C

Supporting Software

A number of software tools were developed in the context of the research presented in this disseratation. These have been written in Python, a modern object-oriented programming language with excellent support for scientific applications [Oli07]. Some of these tools have grown into more polished projects. In the hope that they will be useful to others, they have been documented and published as open-source software. The projects are hosted on GitHub[1], making it easy for others to contribute to their development.

In this appendix, two of these projects are discussed in more detail. The first of these, *Python-nport* is a Python package (or toolbox in MATLAB terms) that greatly simplifies working with n-port data. *Python-substratestack*, also a Python package, aids in working with the substrate definition of an IC process and its use in EM field solvers.

C.1 Python-nport

In circuit theory, n-port network parameters are widely used in modeling both lumped and distributed networks. Often, the behavior of a network is frequency-dependent and is represented by a list of network parameters corresponding to a list of sampled frequency points. This data is typically stored in Touchstone or CITI files, two file formats that are widely supported by EDA tools such as circuit simulators and EM field solvers.

C.1.1 Feature Overview

The Python nport package tries to provide an intuitive interface to n-port network parameter data. The frequency dependence of the parameters is handled transparantly so that the user does not have to take care of it manually. This way, performing calculations on n-port data is simplified significantly. In addition, a large number of functions to manipulate the n-port data are provided. These include functionality for converting between the different n-port representations:

- impedance (Z) parameters
- admittance (Y) parameters

[1] http://github.com/bmachiel

- scattering (S) parameters

A special subset of n-ports are 2n-ports, which are useful in multiconductor transmission line analysis. Supported representations of 2n-ports are those listed above and, additionally:

- transmission (ABCD) parameters
- scattering transfer (T) parameters

Two-port networks support two additional representations:

- hybrid (H) parameters
- inverse hybrid (G) parameters

The scattering and scattering transfer representations require a normalizing impedance Z_0 to be specified, typically 50 Ω.

Next to providing an abstraction for n-port parameter data, the package includes extra modules building on top of this basic functionality:

- reading and writing of Touchstone and CITI files
- transforming n-port data
- combining two or more n-port networks
- checking properties of the n-port such as passivity and stability
- deembedding of (transistor) measurements
- represention of and calculations with multiconductor transmission lines
- Smith chart plotting (including stability circles)

Some of these features are illustrated in the following section.

C.1.2 An Introductory Tutorial

To load n-port data from a Touchstone file, we import the `touchstone` module from `nport`. We also import `nport` for later use:

```
>>> import nport
>>> from nport import touchstone
```

An N-port network is represented as an object of the `NPort` class, which is basically an array of n-port matrices (one for each frequency sample). Similarly, there are the `TwoPort` and `TwoNPort` classes. The `touchstone.read()` function reads the data from a given file and returns an `NPort` object:

```
>>> filter1 = touchstone.read("filter1.s2p")
>>> filter2 = touchstone.read("filter2.s2p")
```

A lot of functionality is contained in the `NPort` methods. The `is_passive()` method checks passivity of the n-port data, for example. The filters `filter1` and `filter2` are two-ports (reflected by the "s2p" filename extensions) and thus objects of the `TwoNPort` class, which has some additional methods, such as for evaluating the stability of the network:

```
>>> filter1.is_passive()
True
>>> filter2.is_stable_mu()
True
>>> filter2.is_conditionally_stable_mu(0.5, 0.2)
True
```

In addition, the stability circles can be plotted using the `stability_circle_source()` and `stability_circle_load()` methods.

Cascading the two filters `filter1` and `filter2` simply requires converting to a `TwoNPort` represented with ABCD parameters and performing matrix dot multiplication:

```
>>> filter1_abcd = filter1.twonport().convert(nport.ABCD)
>>> filter2_abcd = filter2.twonport().convert(nport.ABCD)
>>> filters = nport.dot(filter1_abcd, filter2_abcd)
```

Note that we did not have to worry about the frequency dependence of the data. The frequency samples of `filter1` and `filter2` do not have to coincide. The `nport.dot` function silently performs interpolation and returns a `TwoNPort` defined across the frequency range shared by the two input `TwoNPorts`. The same is true for the (element-wise) binary operations on `NPort` object, such as

```
>>> no_physical_meaning = filter1 + filter2
```

The cascade of the two filters can be written back to a Touchstone file:

```
>>> touchstone.write(filters, "filters")
```

producing a "filters.s2p" file.

When working with network data originating from an EM field solver, it is sometimes required to change the polarity of ports, assign one port as the reference for another or connect two ports toghether. The `NPort.recombine()` and `NPort.shunt()` methods assist in this task. Similarly useful is the `NPort.parallel()` method, which allows to connect two `NPorts` together arbitrarily. This can be used to connect a transistor model to that of a passive structure, for example.

Transmission Lines

Suppose we have simulated a piece of microstrip line of 100 µm length in Momentum and exported the result to a Touchstone file. From the `TwoPort` object, we can generate a `TransmissionLine` object (passing the lenght of the line):

```
>>> mstrip = touchstone.read("mstrip.s2p")
>>> mstrip_tline = mstrip.transmission_line(100e-6)
```

The line's per-unit-length RLGC parameters, propagation constant and characteristic impedance can be obtained by accessing the respective properties of `mstrip_tline`. For example, `mstrip_tline.l` and `mstrip_tline.gamma` respectively hold the per-unit-length inductance and propagation constant of the line.

The `TransmissionLine` object can be transformed back to a `TwoPort`. This requires specifying the length of the line and can thus be used to generate a model of a transmission line with arbitrary length, suitable for use in a circuit simulator:

```
>>> mstrip_275um = mstrip_tline.twoport(275e-6)
>>> touchstone.write(mstrip_275um, "mstrip_275um")
```

The microstrip example above assumes a passive microstrip line. For the simulation of the traveling-wave transistor discussed in Chapter 5, support for non-reciprocal lines was included. This requires passing a value of `False` to the optional `reciprocal` parameter of the `TwoPort.transmission_line()` method. The resulting `TransmissionLine` object then differentiates between properties in the forward and the backward direction; `TransmissionLine.gamma_forward` and `TransmissionLine.gamma_backward` for the propagation constant, for example.

Support for multiconductor transmission lines is also provided, based on the modal analysis theory for non-uniform multiconductor transmission lines by Faria [Far04], and extended for non-reciprocal lines as discussed in Appendix B. This implemenation is used as the basis of the traveling-wave MOSFET explorer show in Figure 5.18.

RF Measurement Deembedding

Deembedding a device under test (DUT) from a measurement fixture typically involves performing numerous calculations on the measured data of the DUT in the fixture and the dummy structures. As Python-nport simplifies calculations with n-port data, these deembedding methods can be implemented relatively easily.

The classic open-short two-step deembedding method requires measurements of open and short dummy structures. The following example illustrates how to create a `TwoStep` deembedder by feeding it the n-port data of the dummy structures. The deembedder is then used to deembed three different NMOS measurements:

```
from nport import touchstone
from nport.deemb import TwoStep

# read in S-parameters of dummy structures
open = touchstone.read("deemb_open.s2p")
```

```
short = touchstone.read("deemb_short.s2p")

# set up the de-embedder
twostep = TwoStep(open, short)

# read in S-parameters of devices
nmos16 = touchstone.read("nmos_W16_L80_Vg10_Vd12.s2p")
nmos32 = touchstone.read("nmos_W32_L80_Vg10_Vd12.s2p")
nmos64 = touchstone.read("nmos_W64_L80_Vg10_Vd12.s2p")

# de-embed the measurements
deemb16 = twostep.deembed(nmos16)
deemb32 = twostep.deembed(nmos32)
deemb64 = twostep.deembed(nmos64)

# write the de-embedded S-parameters to touchstone files
touchstone.write(deemb16, "nmos_W16_L80_Vg10_Vd12_deembedded")
touchstone.write(deemb32, "nmos_W32_L80_Vg10_Vd12_deembedded")
touchstone.write(deemb64, "nmos_W64_L80_Vg10_Vd12_deembedded")
```

In addition to the simple two-step deembedder, implementations of three-step [Van01] and four-step [Kol00] deembedding methods specifically designed for on-wafer transistor measurements are provided. These require more dummy structures but offer better accuracy at higher frequencies. Based on a mathematical description, a new deembedding method can easily be added to Python-nport.

For more information and complete documentation on Python-nport, please visit its homepage[2].

C.2 Python-substratestack

The design of RFIC passives such as planar inductors and transmission lines requires simulations using electromagnetic field solvers such as ADS Momentum and Sonnet em. These require an accurate definition of the substrate stack in order to output correct models of the passive structures. The designer typically manually copies the substrate stack definition from the documentation provided by the IC foundry into the solver by means of its graphical user interface. However, often the stack first needs to be simplified to keep simulation times down. The simplification and manual entry of the stack into the solver is a tedious and error-prone process. Python-substratestack tries to make this process quicker and more robust.

Python-substratestack takes the detailed definition of a substrate stackup describing the oxide and metal layers of an IC technology, as provided in the design kit documentation. Modern CMOS processes have a large number of oxide layers in their back-end-of-line (BEOL) stack. The Python module merges these into an equivalent oxide layer where possible, significantly reducing simulation times. Also, as passive RF components typically do not use all metals in the metal stack, the designer can choose to remove unused metals from the stack. Python-substratestack will then merge the neighboring oxide layers, further reducing simulation times. As the simplification of the stack is

[2] http://bmachiel.github.com/python-nport

performed programmatically rather than manually, this process is much faster and less likely to suffer from mistakes, which can turn out to be very costly in IC design.

The module can also write out a detailed visualization of the stack to a PDF, so that the correct entry of the stack definition can be verified. Finally, the simplified stack definition can be exported to a Momentum SLM file or a Sonnet em project for direct inclusion in these solvers.

C.2.1 An Example

The example below illustrates how the stack definition is entered and simplified. The stack described is that from a hypothetical four-metal-layer CMOS process.

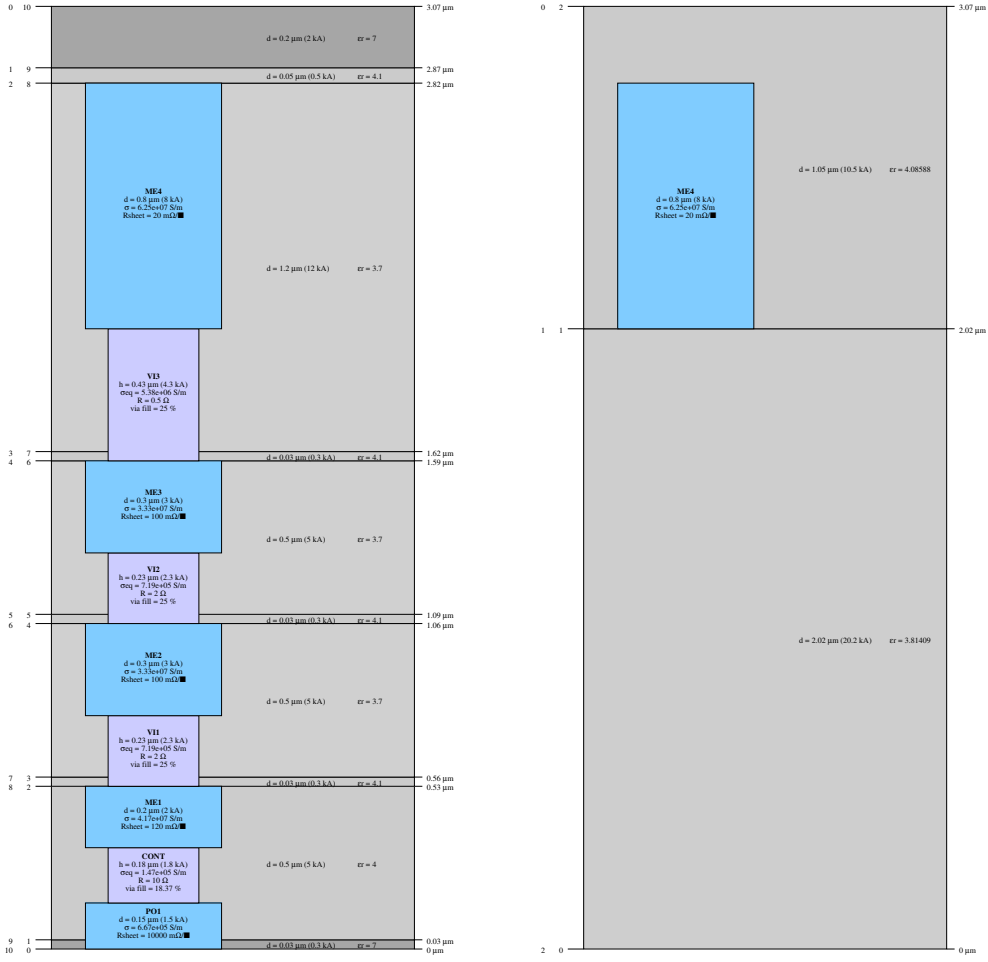
```
# import everything needed from the substratestack module
from substratestack import m, mm, um, A, kA
from substratestack import Ohm_m, Ohm_cm, S_m, Ohm, mOhm, Ohm_sq, mOhm_sq

from substratestack import SubstrateStack
from substratestack import BulkLayer, OxideLayer, MetalLayer, Via, UP, DOWN

# The stack is entered from bottom to top, starting with the bulk.
# BulkLayer arguments: thickness, resistivity, dielectric loss tangent
bulk = BulkLayer(300 * um, 11.9, 20 * Ohm_cm, 0)

# Create a SubstrateStack object using the specified bulk layer.
stack = SubstrateStack(bulk)

# Add all oxide layers to the stack, starting with the bottom one, working
# up to the top.
# OxideLayer arguments: thickness, relative epsilon, loss tangent
stack.add_oxide_layer_on_top(OxideLayer(300 * A, 7, 0))
stack.add_oxide_layer_on_top(OxideLayer(5.0 * kA, 4, 0))
stack.add_oxide_layer_on_top(OxideLayer(300 * A, 4.1, 0))
stack.add_oxide_layer_on_top(OxideLayer(5.0 * kA, 3.7, 0))
stack.add_oxide_layer_on_top(OxideLayer(300 * A, 4.1, 0))
stack.add_oxide_layer_on_top(OxideLayer(5.0 * kA, 3.7, 0))
stack.add_oxide_layer_on_top(OxideLayer(300 * A, 4.1, 0))
stack.add_oxide_layer_on_top(OxideLayer(12 * kA, 3.7, 0))
stack.add_oxide_layer_on_top(OxideLayer(500 * A, 4.1, 0))
stack.add_oxide_layer_on_top(OxideLayer(2 * kA, 7, 0))

# Print the layer stack to example_nometals.pdf to see at what interface number
# the metals should go
stack.draw('example_nometals', pages=1.5)

# Add metal layers
# MetalLayer arguments: name, thickness, sheet resistance, extension direction,
#   interface number
stack.add_metal_layer(MetalLayer('PO1', 1.5 * kA, 10 * Ohm_sq, UP), 0)
stack.add_metal_layer(MetalLayer('ME1', 2.0 * kA, 120 * mOhm_sq, DOWN), 2)
stack.add_metal_layer(MetalLayer('ME2', 3.0 * kA, 100 * mOhm_sq, DOWN), 4)
stack.add_metal_layer(MetalLayer('ME3', 3.0 * kA, 100 * mOhm_sq, DOWN), 6)
stack.add_metal_layer(MetalLayer('ME4', 8 * kA, 20 * mOhm_sq, DOWN), 8)

# Add vias
```

```
# Via arguments: name, resistance, width or height (vias are assumed square),
#   spacing (defaults to 0)
# LayerStack.add_via arguments: via, bottom metal name, top metal name
stack.add_via(Via('CONT', 10 * Ohm, 0.15 * um, 0.20 * um), 'PO1', 'ME1')
stack.add_via(Via('VI1', 2 * Ohm, 0.20 * um, 0.20 * um), 'ME1', 'ME2')
stack.add_via(Via('VI2', 2 * Ohm, 0.20 * um, 0.20 * um), 'ME2', 'ME3')
stack.add_via(Via('VI3', 0.5 * Ohm, 0.20 * um, 0.20 * um), 'ME3', 'ME4')

# Print the full layer stack to example.pdf for verification of the input data
stack.draw('example', pages=1.5)

# Remove all metal layers except for the top metal
stack.remove_metal_layer_by_name('PO1')
stack.remove_metal_layer_by_name('ME1')
stack.remove_metal_layer_by_name('ME2')
stack.remove_metal_layer_by_name('ME3')

# Merge oxide layers to reduce the stack's complexity, speeding up simulation
stack.simplify()

# Print the simplified stack to example_ME4.pdf
stack.draw('example_ME4', pages=1.5)

# Write out a Momentum subtrate definition file of the simplified stack
stack.write_momentum_substrate('example_ME4')

# Write out a Sonnet project that includes the simplified subtrate stack
stack.write_sonnet_technology('example_ME4')
```

Two of the PDF files output by the progam above, `example.pdf` and `example_ME4.pdf`, are shown in Figure C.1. It shows how the stack is simplified to only two oxide layers and a single metal layer.

This simplified example does not illustrate the full funcionality of the substratestack module. A more detailed example can be explored at the interactive demo website[3].

[3] https://substratestack.appspot.com/



(a) (b)

Figure C.1: Substrate stack as rendered by the Python substratestack module: (a) full, and (b) simplified.

List of Publications

Papers in international journals

- B. Machiels, P. Reynaert and M. Steyaert, "The Tapered Matrix Amplifier: A Low-Power High-Gain Broadband Amplifier", *Analog Integrated Circuits and Signal Processing*, accepted for publication.

Papers in international conference proceedings

- B. Machiels, P. Reynaert and M. Steyaert, "Linearity-enhanced low-power distributed low-noise amplifier in CMOS", *ICT.OPEN, November 2011.*
- B. Machiels, P. Reynaert and M. Steyaert, "Power efficient distributed low-noise amplifier in 90 nm CMOS", *IEEE Radio Frequency Integrated Circuits Symposium (RFIC), 2010.*
- M. Steyaert, F. Gobert, L. Li, B. Machiels and P. Reynaert "RF-CMOS: Analog Circuits and Digital Techniques", *Ph.D. Research in Microelectronics and Electronics (PRIME), June 2008.*

Bibliography

[Aga98] B. Agarwal, A.E. Schmitz, J.J. Brown, M. Matloubian, M.G. Case, M. Le, M. Lui, and M.J.W. Rodwell, "112-GHz, 157-GHz, and 180-GHz InP HEMT traveling-wave amplifiers", *Microwave Theory and Techniques, IEEE Transactions on*, vol. 46, no. 12, pp. 2553 –2559, dec 1998.

[Agia] Agilent, "10 hints for making successful noise figure measurements", *Application Note 57-3*.

[Agib] Agilent, "Fundamentals of RF and microwave noise figure measurements", *Application Note 57-1*.

[Agic] Agilent, "Noise figure measurement accuracy - the Y-factor method", *Application Note 57-2*.

[Ahn02] H.T. Ahn, DJ Allstot, Q. Inc, and CA San Diego, "A 0.5-8.5 GHz fully differential CMOS distributed amplifier", *Solid-State Circuits, IEEE Journal of*, vol. 37, no. 8, pp. 985–993, 2002.

[Ait85] CS Aitchison, "The intrinsic noise figure of the MESFET distributed amplifier", *Microwave Theory and Techniques, IEEE Transactions on*, vol. 33, no. 6, pp. 460–466, 1985.

[Ait01] C.S. Aitchison and M. Mbabele, "Third order intermodulation improvement in distributed amplifiers", in *Microwave Conference, 2001. 31st European*, pp. 1 –4, sept. 2001.

[And96] D. Anderson, L. Smith, and J. Gruszynski, "S-parameter techniques for faster, more accurate network design", *Test and Measurement Application Note, Hewlett-Packard Company, USA*, vol. 1997, pp. 4–13, 1996.

[And03] S. Andersson, C. Svenson, and O. Drugge, "Wideband LNA for a multistandard wireless receiver in 0.18 m CMOS", in *Solid-State Circuits Conference, 2003. ESSCIRC '03. Proceedings of the 29th European*, sept. 2003.

[Anra] Anritsu, "Noise figure", *Application Note*.

[Anrb] Anritsu, "Noise figure corrections", *Application Note*.

[Aok08] I. Aoki, S. Kee, R. Magoon, R. Aparicio, F. Bohn, J. Zachan, G. Hatcher, D. McClymont, and A. Hajimiri, "A fully-integrated quad-band gsm/gprs cmos power amplifier", *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 12, pp. 2747 –2758, dec. 2008.

[Arb08] A. Arbabian and A.M. Niknejad, "A broadband distributed amplifier with internal feedback providing 660ghz gbw in 90nm cmos", *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, pp. 196–197, 2008.

[Arb09] A. Arbabian and A.M. Niknejad, "Design of a CMOS tapered cascaded multistage distributed amplifier", *Microwave Theory and Techniques, IEEE Transactions on*, vol. 57, no. 4, pp. 938–947, April 2009.

[Bae06] Y. Baeyens, N. Weimann, V. Houtsma, J. Weiner, Y. Yang, J. Frackoviak, P. Roux, A. Tate, and Y.K. Chen, "Submicron InP D-HBT single-stage distributed amplifier with 17 dB gain and over 110 GHz bandwidth", in *Microwave Symposium Digest, 2006. IEEE MTT-S International*, june 2006.

[Bak06] R.A. Baki, T.K.K. Tsang, and M.N. El-Gamal, "Distortion in RF CMOS short-channel low-noise amplifiers", *Microwave Theory and Techniques, IEEE Transactions on*, vol. 54, no. 1, pp. 46–56, Jan. 2006.

[Ban00] BY Banyamin and M. Berwick, "Analysis of the performance of four-cascaded single-stage distributed amplifiers", *Microwave Theory and Techniques, IEEE Transactions on*, vol. 48, no. 12, pp. 2657–2663, 2000.

[Ber93] C. Berrou, A. Glavieux, and P. Thitimajshima, "Near shannon limit error-correcting coding and decoding: Turbo-codes (1)", in *Communications, 1993. ICC 93. Geneva. Technical Program, Conference Record, IEEE International Conference on*, volume 2, may 1993.

[Bev04] A. Bevilacqua and AM Niknejad, "An ultrawideband CMOS low-noise amplifier for 3.1-10.6-GHz wireless receivers", *Solid-State Circuits, IEEE Journal of*, vol. 39, no. 12, pp. 2259–2268, 2004.

[Bey84] JB Beyer, SN Prasad, RC Becker, JE Nordman, and GK Hohenwarter, "MESFET distributed amplifier design guidelines", *Microwave Theory and Techniques, IEEE Transactions on*, vol. 32, no. 3, pp. 268–275, 1984.

[Boh08] Keefe Bohannan, Jeannick Sercu, and John Moore, "Demystifying ports & grounds in ADS Momentum", September 2008, Rev 1.1.

[BT80] C.R. Brewitt-Taylor, P.N. Robson, and J.E. Sitch, "Noise figure of m.e.s.f.e.t.s", *Solid-State and Electron Devices, IEE Proceedings I*, vol. 127, no. 1, pp. 1 –8, february 1980.

[Che05] Xu Chen and Zhigong Wang, "Design of 0.1 sim;14 ghz fully-integrated tapered distributed amplifiers in 0.25 mu;m cmos", in *Microwave Conference Proceedings, 2005. APMC 2005. Asia-Pacific Conference Proceedings*, volume 2, page 4 pp., dec. 2005.

[Che07] Hsien-Ku Chen, Da-Chiang Chang, Ying-Zong Juang, and Shey-Shi Lu, "A compact wideband CMOS low-noise amplifier using shunt resistive-feedback and series inductive-peaking techniques", *Microwave and Wireless Components Letters, IEEE*, vol. 17, no. 8, pp. 616 –618, aug. 2007.

[Che09] M. Chen and J. Lin, "A 0.1-20 GHz low-power self-biased resistive-feedback LNA in 90 nm digital CMOS", *Microwave and Wireless Components Letters, IEEE*, vol. 19, no. 5, pp. 323 –325, may. 2009.

[Che10] Jiashu Chen and A.M. Niknejad, "A stage-scaled distributed power amplifier achieving 110GHz bandwidth and 17.5dBm peak output power", in *Radio Frequency Integrated Circuits Symposium (RFIC), 2010 IEEE*, pp. 347 –350, May 2010.

[Chi07] J.C. Chien and L.H. Lu, "40-Gb/s high-gain distributed amplifiers with cascaded gain stages in 0.18-um CMOS", *Solid-State Circuits, IEEE Journal of*, vol. 42, no. 12, pp. 2715–2725, 2007.

[Col01] RE Collin, *Foundations for Microwave Engineering*, IEEE Press, 2001.

[Col02] J.-M. Collantes, R.D. Pollard, and M. Sayed, "Effects of dut mismatch on the noise figure characterization: a comparative analysis of two y-factor techniques", *Instrumentation and Measurement, IEEE Transactions on*, vol. 51, no. 6, pp. 1150 – 1156, dec 2002.

[Cor03] Steve Corey, "Re: N-port model limitations in simulators", Signal Integrity List (si-list), April 28 2003, http://www.freelists.org/post/si-list/Nport-model-limitations-in-simulators,16.

[Cou97] L.W. Couch, *Digital and Analog Communication Systems*, Prentice-Hall, Upper Saddle River, NJ, 1997.

[D'E] John D'Errico, "Eigenshuffle", `http://www.mathworks.com/matlabcentral/fileexchange/22885-eigenshuffle`.

[Dor01] R.C. Dorf and R.H. Bishop, *Modern Control Systems*, Prentice Hall, 9 edition, 2001.

[Dup10] J.-Y. Dupuy, A. Konczykowska, F. Jorge, M. Riet, and J. Godin, "Distributed amplifiers in InP DHBT for 100-Gbit/s operation", in *Microwave Symposium Digest (MTT), 2010 IEEE MTT-S International*, pp. 920 –923, may 2010.

[Far93] J.A.B. Faria, *Multiconductor transmission-line structures: modal analysis techniques*, Wiley-Interscience, 1993.

[Far94] M. Farina, G. Gerini, and T. Rozzi, "A new technique for the field analysis of active FET devices", volume 1, pp. 865 –869, sept. 1994.

[Far95] M. Farina, L. Pierantoni, and T. Rozzi, "Field analysis and design criteria for T-gate TW-FET's with positive gain", pp. 1269 –1272 vol.3, may 1995.

[Far97a] M. Farina, A. Morini, L. Pierantoni, and T. Rozzi, "Electromagnetic investigation on the propagation in distributed active devices", *Microwaves, Antennas and Propagation, IEE Proceedings* -, vol. 144, no. 5, pp. 281 –288, oct 1997.

[Far97b] M. Farina and T. Rozzi, "A theory of distributed amplifiers exploiting growing waves", in *Microwave Symposium Digest, 1997., IEEE MTT-S International*, volume 2, 1997.

[Far04] J.A.B. Faria, "A new generalized modal analysis theory for nonuniform multiconductor transmission lines", *Power Systems, IEEE Transactions on*, vol. 19, no. 2, pp. 926–933, May 2004.

[Fri44] HT Friis, "Noise figures of radio receivers", *Proceedings of the IRE*, vol. 32, no. 7, pp. 419–422, 1944.

[Fya97] R.S. Fyath, Khaeria A.M. Ali, and R.F. Khalid, "An alternative way to analyse non-reciprocal and non-symmetric transmission lines.", *International Journal of Electronics*, vol. 83, no. 5, pp. 623, 1997.

[Gin48] E.L. Ginzton, W.R. Hewlett, J.H. Jasberg, and J.D. Noe, "Distributed amplification", *Proceedings of the IRE*, vol. 36, no. 8, pp. 956–969, aug 1948.

[Goo02] Jung-Suk Goo, Hee-Tae Ahn, D.J. Ladwig, Zhiping Yu, T.H. Lee, and R.W. Dutton, "A noise optimization technique for integrated low-noise amplifiers", *Solid-State Circuits, IEEE Journal of*, vol. 37, no. 8, pp. 994 – 1002, aug 2002.

[Gra01] P.R. Gray, P.J. Hurst, S.H. Lewis, and R.G. Meyer, *Analysis and design of analog integrated circuits*, Wiley, 4 edition, 2001.

[Han90] K. Han and T.T.Y. Wong, "Coupled-wave small-signal transient analysis of GaAs distributed amplifier", *Microwave Theory and Techniques, IEEE Transactions on*, vol. 38, no. 1, pp. 23 –29, jan 1990.

[Hei83] W. Heinrich and H.L. Hartnagel, "Wave-theoretical analysis of signal propagation on FET electrodes", *Electronics Letters*, vol. 19, no. 2, pp. 65–67, January 1983.

[Hei86] W. Heinrich, "Limits of FET modelling by lumped elements", *Electronics Letters*, vol. 22, no. 12, pp. 630–632, June 1986.

[Hei87a] W. Heinrich, "Distributed equivalent-circuit model for traveling-wave FET design", *Microwave Theory and Techniques, IEEE Transactions on*, vol. 35, no. 5, pp. 487–491, 1987.

[Hei87b] W. Heinrich and HL Hartnagel, "Wave propagation on MESFET electrodes and its influence on transistor gain", *Microwave Theory and Techniques, IEEE Transactions on*, vol. 35, no. 1, pp. 1–8, 1987.

[Hey07] P. Heydari, "Design and analysis of a performance-optimized CMOS UWB distributed LNA", *Solid-State Circuits, IEEE Journal of*, vol. 42, no. 9, pp. 1892–1905, 2007.

[Hin70] M.E. Hines, "A new microstrip isolator and its application to distributed diode amplification", in *Microwave Symposium, G-MTT 1970 International*, pp. 304 –307, may 1970.

[Hol84] AJ Holden and CH Oxley, "Computer modelling of travelling wave transistors", *Proc. Int. Conf. Simulation of Semiconductor Devices and Pocesses*, pp. 319–326, July 1984.

[Hol85] A.J. Holden, D.R. Daniel, I. Davies, C.H. Oxley, and H.D. Rees, "Gallium arsenide traveling-wave field-effect transistors", *Electron Devices, IEEE Transactions on*, vol. 32, no. 1, pp. 61–66, Jan 1985.

[Hua99] Qiuting Huang, P. Orsatti, and F. Piazza, "GSM transceiver front-end circuits in 0.25-um CMOS", *Solid-State Circuits, IEEE Journal of*, vol. 34, no. 3, pp. 292 –303, mar 1999.

[Ism04] A. Ismail and AA Abidi, "A 3-10-GHz low-noise amplifier with wideband LC-ladder matching network", *Solid-State Circuits, IEEE Journal of*, vol. 39, no. 12, pp. 2269–2277, 2004.

[Jan01] Johan Janssens, *Deep Submicron CMOS Cellular Receiver Front-ends*, PhD thesis, Katholieke Universiteit Leuven, jul 2001.

[Jut68] W. Jutzi, "Uniform distributed amplifier analysis with fast and slow waves", *Proceedings of the IEEE*, vol. 56, no. 1, pp. 66–67, 1968.

[Kim04] Jonghae Kim, J.-O. Plouchart, N. Zamdmer, R. Trzcenski, R. Groves, M. Sherony, Y. Tan, M. Talbi, J. Safran, and L. Wagner, "A 12dbm 320ghz gbw distributed amplifier in a 0.12 mu;m soi cmos", in *Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International*, pp. 478 – 540 Vol.1, feb. 2004.

[Ko05] Won Ko and Youngwoo Kwon, "Improved noise analysis of distributed preamplifier with cascode FET cells", *Microwave Theory and Techniques, IEEE Transactions on*, vol. 53, no. 1, pp. 361 – 371, jan. 2005.

[Koh68] G. Kohn and R.W. Landauer, "Distributed field-effect amplifiers", *Proceedings of the IEEE*, vol. 56, no. 6, pp. 1136–1137, June 1968.

[Kol00] TE Kolding, "A four-step method for de-embedding gigahertz on-wafer CMOS measurements", *Electron Devices, IEEE Transactions on*, vol. 47, no. 4, pp. 734–740, 2000.

[Kom72] R. Kompfner, "Optics at bell laboratories—optical communications", *Applied Optics*, vol. 11, no. 11, pp. 2412–2425, Nov 1972.

[Kop66] E.H. Kopp, "A coupled mode analysis of the traveling-wave transistor", *Proceedings of the IEEE*, vol. 54, no. 11, pp. 1571–1572, Nov. 1966.

[Lee04a] T.H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, 2004.

[Lee04b] T.H. Lee, *Planar Microwave Engineering: A Practical Guide to Theory, Measurement, and Circuits*, Cambridge University Press, 2004.

[Lim03] Wei Meng Lim, Manh Anh Do, Jian Guo Ma, and Kiat Seng Yeo, "A broadband CMOS LNA for WLAN applications", in *Ultra Wideband Systems and Technologies, 2003 IEEE Conference on*, pp. 42 – 46, nov. 2003.

[Lin94] I.V. Lindell, M.E. Valtonen, and A.H. Sihvola, "Theory of nonreciprocal and nonsymmetric uniform transmission lines", *Microwave Theory and Techniques, IEEE Transactions on*, vol. 42, no. 2, pp. 291 –297, feb 1994.

[Liu04] R.C. Liu, C.S. Lin, K.L. Deng, and H. Wang, "Design and analysis of DC-to-14-GHz and 22-GHz CMOS cascode distributed amplifiers", *Solid-State Circuits, IEEE Journal of*, vol. 39, no. 8, pp. 1370–1374, 2004.

[Liu05] R.C. Liu, T.P. Wang, L.H. Lu, H. Wang, S.H. Wang, and C.P. Chao, "An 80GHz travelling-wave amplifier in a 90nm CMOS technology", in *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International*, pp. 154–156, 2005.

[Mac12] Brecht Machiels, Patrick Reynaert, and Michiel Steyaert, "The tapered matrix amplifier: A low-power high-gain broadband amplifier", *Analog Integrated Circuits and Signal Processing*, 2012, accepted for publication.

[Mas53a] SJ Mason, "Feedback theory-some properties of signal flow graphs", *Proceedings of the IRE*, vol. 41, no. 9, pp. 1144–1156, 1953.

[Mas53b] S.J. Mason, *Power Gain in Feedback Amplifiers*, Massachusetts Institute of Technology, Research Laboratory of Electronics, 1953.

[Mas56] SJ Mason, "Feedback theory-further properties of signal flow graphs", *Proceedings of the IRE*, vol. 44, no. 7, pp. 920–926, 1956.

[Mas03] S. Masuda, T. Takahashi, and K. Joshin, "An over-110-GHz InP HEMT flip-chip distributed baseband amplifier with inverted microstrip line structure for optical transmission system", *Solid-State Circuits, IEEE Journal of*, vol. 38, no. 9, pp. 1479 – 1484, sept. 2003.

[McI65] GW McIver, "A traveling-wave transistor", *Proceedings of the IEEE*, vol. 53, no. 11, pp. 1747–1748, 1965.

[Moe08] K. Moez and MI Elmasry, "A low-noise CMOS distributed amplifier for ultra-wide-band applications", *Circuits and Systems II: Express Briefs, IEEE Transactions on [see also Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on]*, vol. 55, no. 2, pp. 126–130, 2008.

[Nic87] K.B. Niclas and R.R. Pereira, "The matrix amplifier: A high-gain module for multioctave frequency bands", *Microwave Theory and Techniques, IEEE Transactions on*, vol. 35, no. 3, pp. 296 – 306, mar 1987.

[Oku09] M. Okushima, J. Borremans, D. Linten, and G. Groeseneken, "A DC-to-22 GHz 8.4mW compact dual-feedback wideband LNA in 90 nm digital CMOS", in *Radio Frequency Integrated Circuits Symposium, 2009. RFIC 2009. IEEE*, pp. 295 –298, June 2009.

[Oli07] Travis E. Oliphant, "Python for scientific computing", *Computing in Science & Engineering*, vol. 9, pp. 10–20, 2007.

[Orf04] Sophocles J. Orfanidis, *Electromagnetic Waves and Antennas*, 2004.

[Pai72] S.F. Paik, "Iterated solid-state microwave power amplifier", *Microwave Theory and Techniques, IEEE Transactions on*, vol. 20, no. 3, pp. 202 – 209, mar 1972.

[Par06a] Jinho Park and D.J. Allstot, "A matrix amplifier in 0.18-um SOI CMOS", *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 53, no. 3, pp. 561 –568, march 2006.

[Par06b] Yunseo Park, Chang-Ho Lee, J.D. Cressler, and J. Laskar, "The analysis of UWB SiGe HBT LNA for its noise, linearity, and minimum group delay variation", *Microwave Theory and Techniques, IEEE Transactions on*, vol. 54, no. 4, pp. 1687 – 1697, june 2006.

[Pau08] C.R. Paul, *Analysis of multiconductor transmission lines*, Wiley-IEEE, 2008.

[Paw06] A.H. Pawlikiewicz and D. Hess, "Choosing RF CMOS or SiGe BiCMOS in mixed-signal design", *RF DESIGN*, vol. 29, no. 3, pp. 36, 2006.

[Per36] W.S. Percival, "Improvements in and Relating to Thermionic Valve Circuits", July 1936, British Patent Specification no. 460,562.

[Pod82] AS Podgorski and LY Wei, "Theory of traveling-wave transistors", *Electron Devices, IEEE Transactions on*, vol. 29, no. 12, pp. 1845–1853, 1982.

[Poz05] D.M. Pozar, *Microwave Engineering*, John Wiley & Sons, Inc, 3rd edition, 2005.

[Raz01] B. Razavi, *Design of analog CMOS integrated circuits*, McGraw-Hill Boston, MA, 2001.

[Rod09] J. Roderick and H. Hashemi, "A 0.13 um CMOS power amplifier with ultra-wide instantaneous bandwidth for imaging applications", in *Solid-State Circuits Conference - Digest of Technical Papers, 2009. ISSCC 2009. IEEE International*, pp. 374 –375,375a, feb. 2009.

[Row64a] HE Rowe, "Imperfections in active transmission lines", *The Bell System technical journal*, vol. 43, pp. 293, 1964.

[Row64b] HE Rowe, "Stability of active transmission lines with arbitrary imperfections", *The Bell System technical journal*, vol. 43, no. 1-4, pp. 293, 1964.

[San06] Willy M. C. Sansen, *Analog Design Essentials*, Springer-Verlag New York, Inc., Secaucus, NJ, USA, 2006.

[Sch00] Rohde & Schwarz, *R&S FS-K3 Software for Measurement of Noise Figure and Gain*, version 3 edition, aug 2000, 1057.3028.02.

[Sch06] A.J. Scholten, R. van Langevelde, L.F. Tiemeijer, and D.B.M. Klaassen, "Compact modeling of noise in CMOS", in *Custom Integrated Circuits Conference, 2006. CICC '06. IEEE*, pp. 711 –716, sept. 2006.

[Seb89] N. Sebati, P. Gamand, C. Varin, F. Pasqualini, and J.-C. Meunier, "Continuous active t-gate travelling-wave transistor", *Electronics Letters*, vol. 25, no. 6, pp. 403 –404, march 1989.

[Sil84] S. Silver, *Microwave antenna theory and design*, IEE electromagnetic waves series. P. Peregrinus on behalf of the Institution of Electrical Engineers, 1984.

[Str03] S. Stroh, "Ultra-wideband: Multimedia unplugged", *IEEE Spectrum*, vol. 40, no. 9, pp. 23–27, 2003.

[Swa03] D.G. Swanson and W.J.R. Hoefer, *Microwave Circuit Modeling Using Electromagnetic Field Simulation*, Artech House, 2003.

[Tec06] Agilent Technologies, *Momentum*, September 2006.

[Ted94] S. Tedja, J. Van der Spiegel, and H.H. Williams, "Analytical and experimental studies of thermal noise in MOSFET's", *Electron Devices, IEEE Transactions on*, vol. 41, no. 11, pp. 2069 –2075, nov 1994.

[Too04] B. Toole, C. Plett, and M. Cloutier, "RF circuit implications of moderate inversion enhanced linear region in MOSFETs", *Circuits and Systems I: Regular Papers, IEEE Transactions on [see also Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on]*, vol. 51, no. 2, pp. 319–328, 2004.

[Tsa04] Ming-Da Tsai, Kuo-Liang Deng, Huei Wang, Chun-Hung Chen, Chih-Sheng Chang, and J.G.J. Chern, "A miniature 25-GHz 9-dB CMOS cascaded single-stage distributed amplifier", *Microwave and Wireless Components Letters, IEEE*, vol. 14, no. 12, pp. 554–556, 2004.

[Tsa05] Ming-Da Tsai, Huei Wang, Jui-Feng Kuan, and Chih-Sheng Chang, "A 70GHz cascaded multi-stage distributed amplifier in 90nm CMOS technology", *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International*, pp. 402–404, 2005.

[Tsi99] Y. Tsividis, *Operation and Modeling of the MOS Transistor*, McGraw-Hill, Inc., 2nd edition, 1999.

[Van01] EP Vandamme, D.M.M.P. Schreurs, G. Van Dinther, and L. IMEC, "Improved three-step de-embedding method to accurately account for the influence of pad parasitics in silicon on-wafer RF test-structures", *Electron Devices, IEEE Transactions on*, vol. 48, no. 4, pp. 737–742, 2001.

[vdZ62] A. van der Ziel, "Thermal noise in field-effect transistors", *Proceedings of the IRE*, vol. 50, no. 8, pp. 1808 –1812, aug. 1962.

[vdZ63] A. van der Ziel, "Gate noise in field effect transistors at moderately high frequencies", *Proceedings of the IEEE*, vol. 51, no. 3, pp. 461 – 467, march 1963.

[Wan11] Beibei Wang and K.J.R. Liu, "Advances in cognitive radio networks: A survey", *Selected Topics in Signal Processing, IEEE Journal of*, vol. 5, no. 1, pp. 5 –23, feb. 2011.

[Wei83] Ce-Jun Wei, "Novel design of travelling-wave FET", *Electronics Letters*, vol. 19, no. 13, pp. 461 –463, June 1983.

[Wik] "Wikipedia: Integrated circuit", `http://en.wikipedia.org/wiki/Integrated_circuit`, Accessed: 19/05/2012.

[Wu05] Chang-Ching Wu, Mei-Fen Chou, Wen-Shen Wuen, and Kuei-Ann Wen, "A low power CMOS low noise amplifier for ultra-wideband wireless applications", in *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on*, pp. 5063 – 5066 Vol. 5, may 2005.

[Zha06] F. Zhang and PR Kinget, "Low-power programmable gain CMOS distributed LNA", *Solid-State Circuits, IEEE Journal of*, vol. 41, no. 6, pp. 1333–1343, 2006.

Biography

Brecht Machiels was born in Genk, Belgium, in 1982. He received the Master of Science in Industrial Sciences (ing.) degree in Electrical Engineering from GroepT, Leuven, Belgium, in 2004. The subject of his thesis was hardware accelerated LabVIEW VIs on FPGA. In the summer of 2006, he completed a six-week internship at AnSem encompassing the design of a passive UHF RFID tag. In 2007, he received the degree of Master of Science in Electrical Engineering (ir.) from the KU Leuven, Belgium. The subject of his thesis was the co-design of a class-E power amplifier and a spread-spectrum switched power supply. From October 2007 to March 2012, he was a research assistant at the MICAS laboratories of the KU Leuven where he was working towards a Ph.D. degree on distributed amplifiers.